

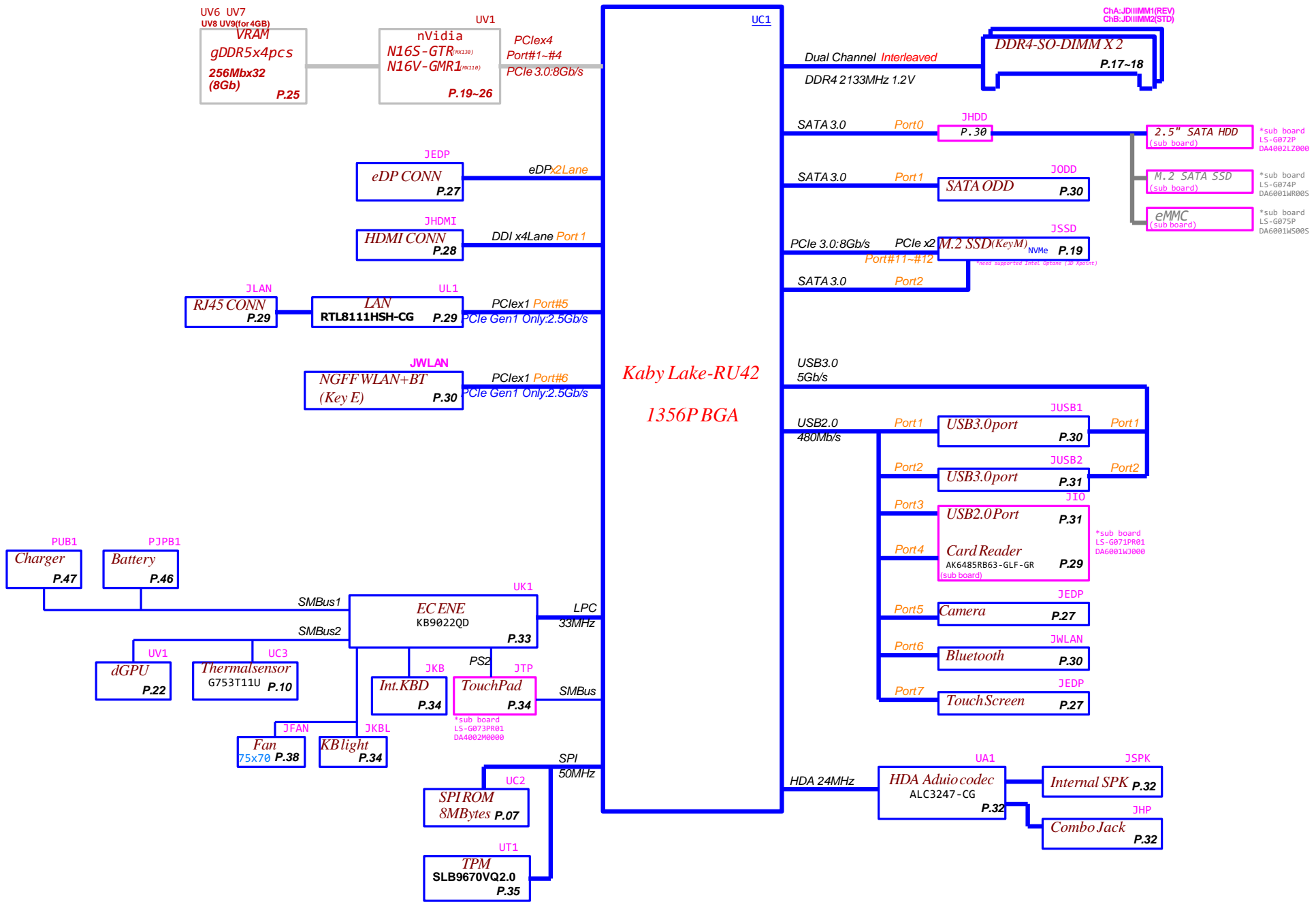
Compal Confidential

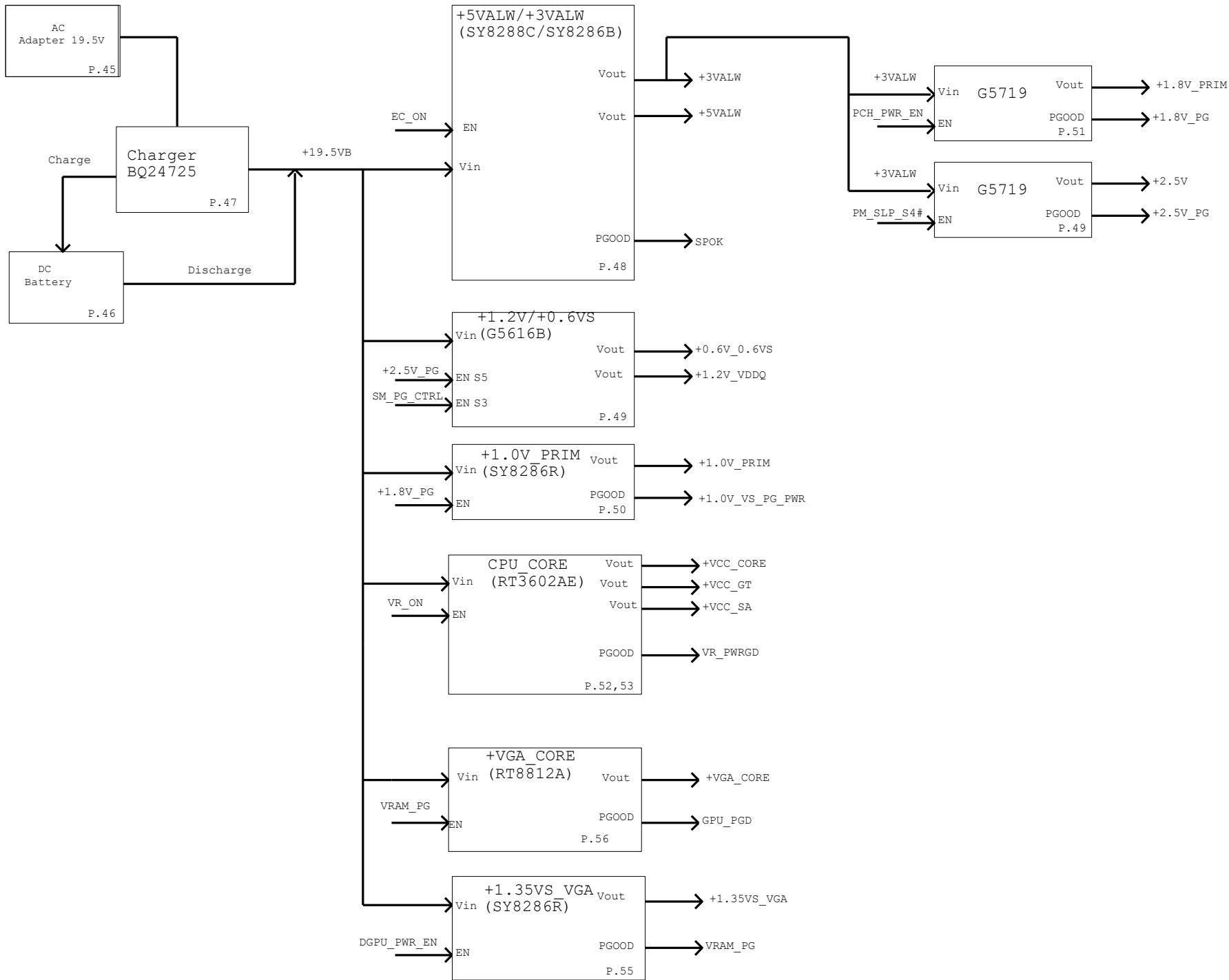
Intel M/B Schematics Document
Kabylake-U(2+2)-DDR4 SODIMMx2
nVidia N16G DDR5-2GB
Project :2018OPP_Harry Potter(15.6")
EPK50 :LA-G07CP

Date : 2018-01-08

REV : 1.0

| | | | | | |
|---|------------|--------------------|------------|--------------------------|--------------------------|
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| Issued Date | 2015/10/22 | Deciphered Date | 2017/10/22 | Title | Cover Page |
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| | | | | Date | Monday, January 08, 2018 |
| | | | | Sheet | 1 of 59 |
| | | | | Rev | v0.3 |



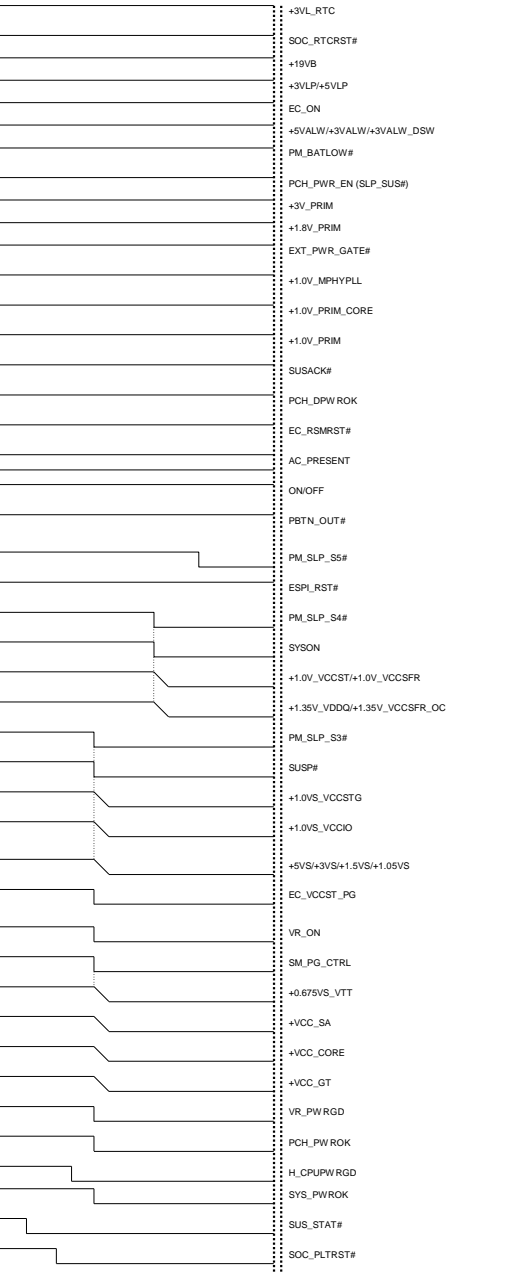
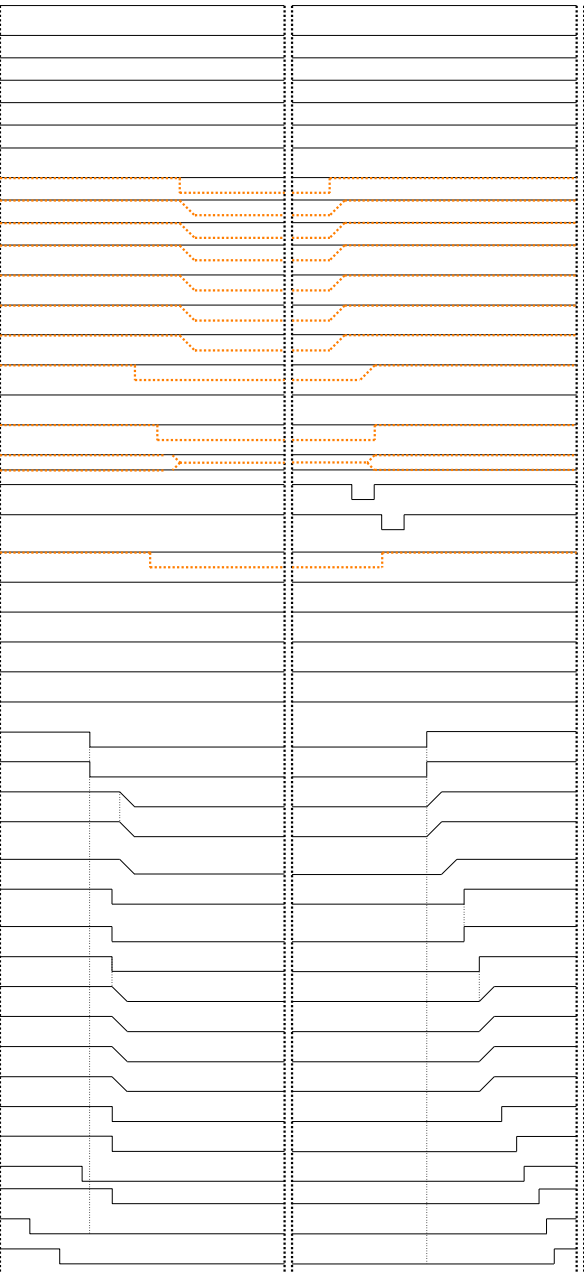
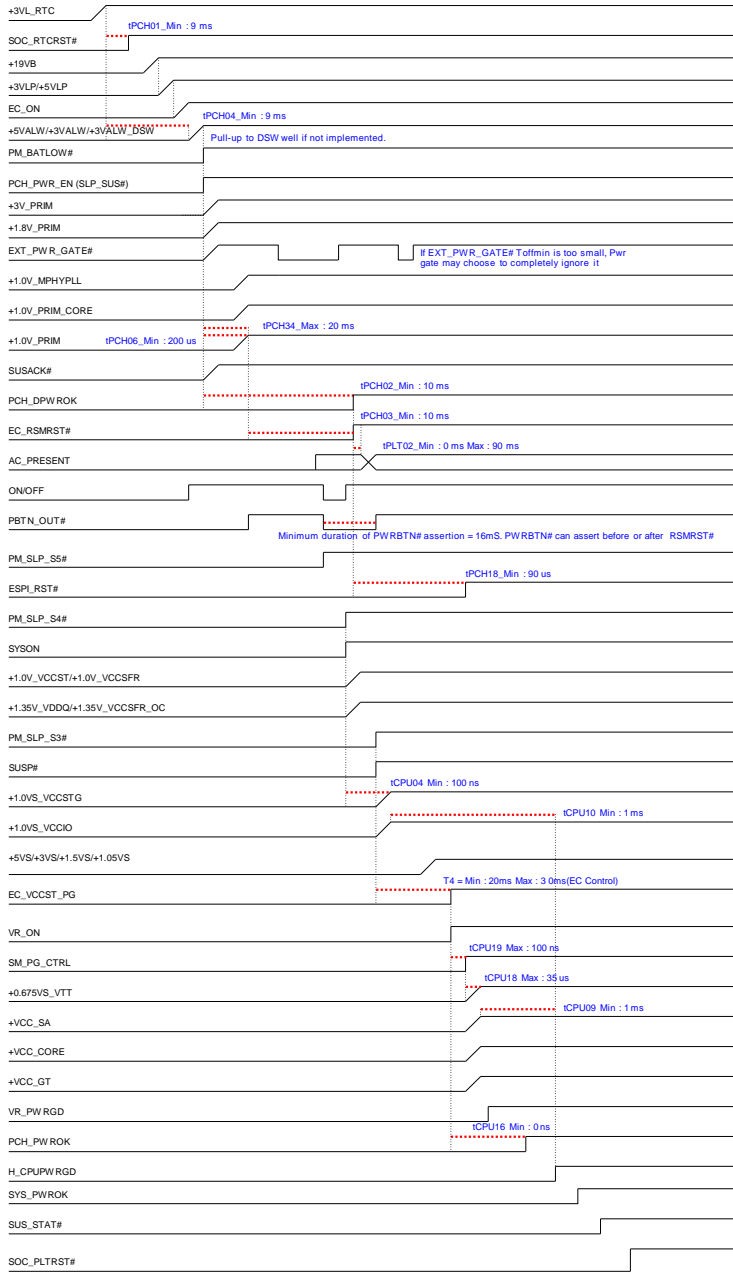


G3->S0

S0->S3/DS3

S0/DS3->S0

S0->S5



SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

1 = Port B is detected.

SOC_DP2_CTRL_DATA(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.

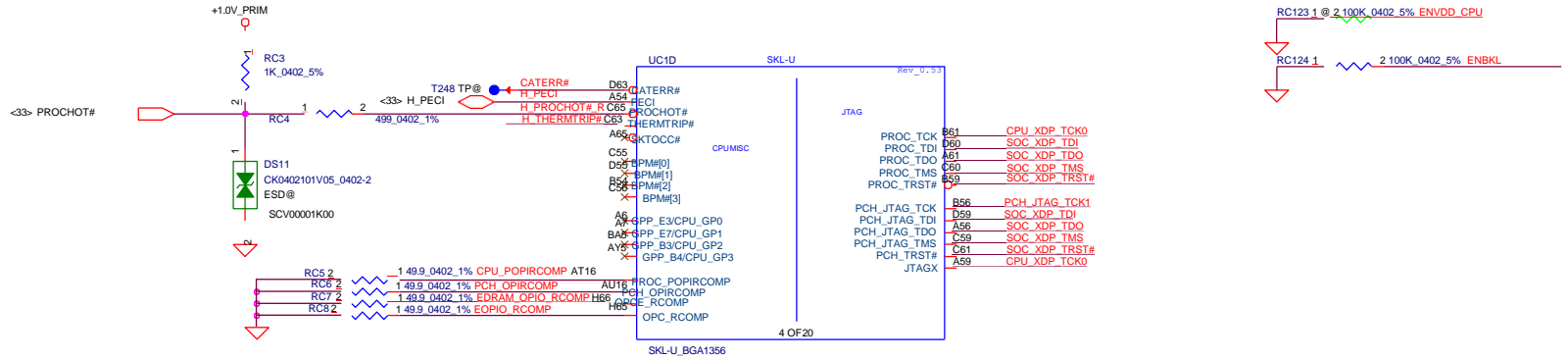
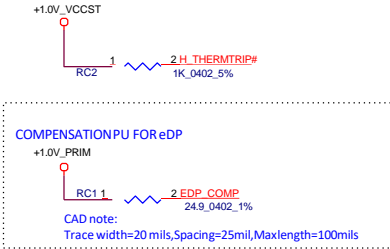
HDMI DDC (Port B)

<28> HOST_DP1_CTRL_CLK
<28> HOST_DP1_CTRL_DATA

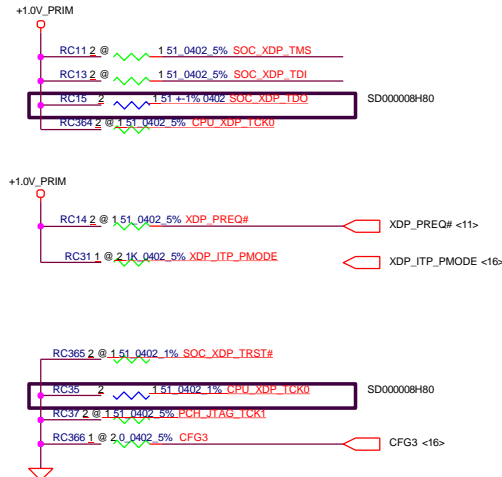
HOST_DP1_CTRL_CLK L13
HOST_DP1_CTRL_DATA L12
GPP_E18/DDPB_CTRLCLK
GPP_E19/DDPB_CTRLDATA
GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA
GPP_E22/DDPD_CTRLCLK
GPP_E23/DDPD_CTRLDATA

1 OF 20

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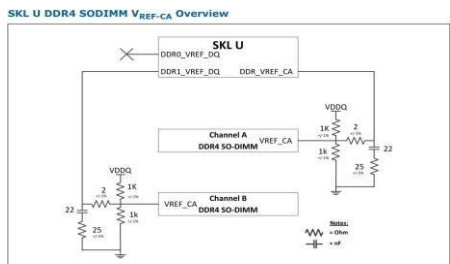
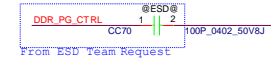
XDP CONN



| Security Classification | Compal SecretData | | Title | |
|--|-------------------|-----------------|------------|-----------------------------|
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| Date: Friday, January 05, 2018 | | | | Rev v0.3 |

Interleaved Memory

PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)

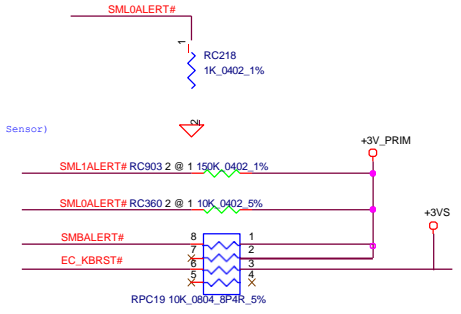


| | | | | |
|--|--------------------|-----------------|---|-----------------------------------|
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| Issued Date | 2017/04/10 | Deciphered Date | 2019/12/15 | Title <i>SKL-U(2/12)DDRIII</i> |
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| | | | Date: Friday, January 05, 2018 | Sheet 6 of 58 |

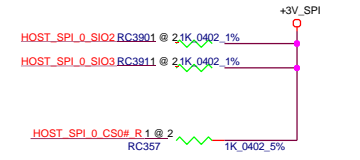
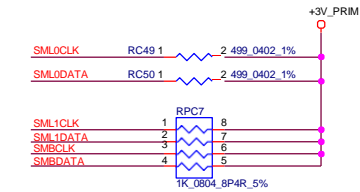
SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC -> For KB9022/9032 Use 1
= eSPI is selected for EC -> For KB9032 Only.

SMB
(Link to XDP, DDR, TP)

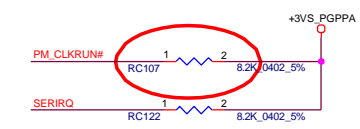
SML1
(Link to EC, DGPU, LAN, Thermal Sensor)



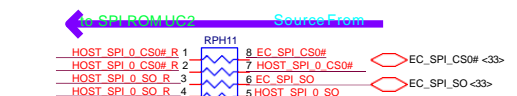
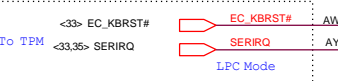
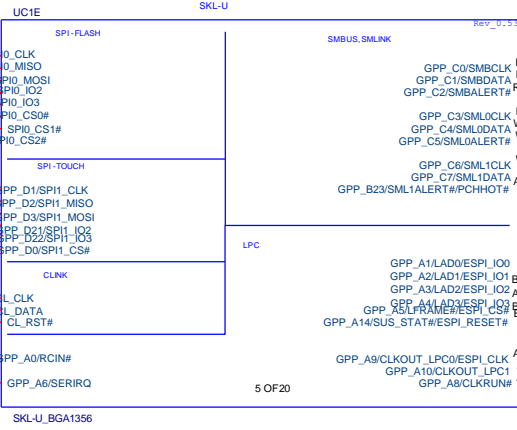
To EC



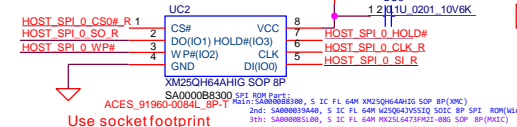
From WW36 MOW for SKL-U ESsample



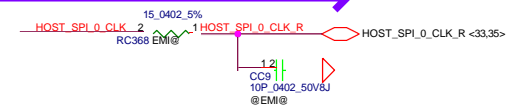
Follow 543016_SKL_U_Y_PDG_0_9



SPI ROM (8MByte Only)

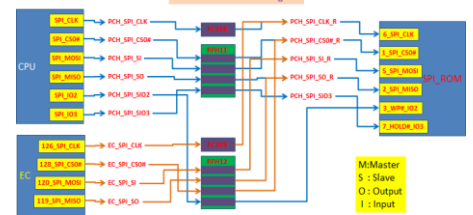


CLK Source CPU to SPI ROM CLK



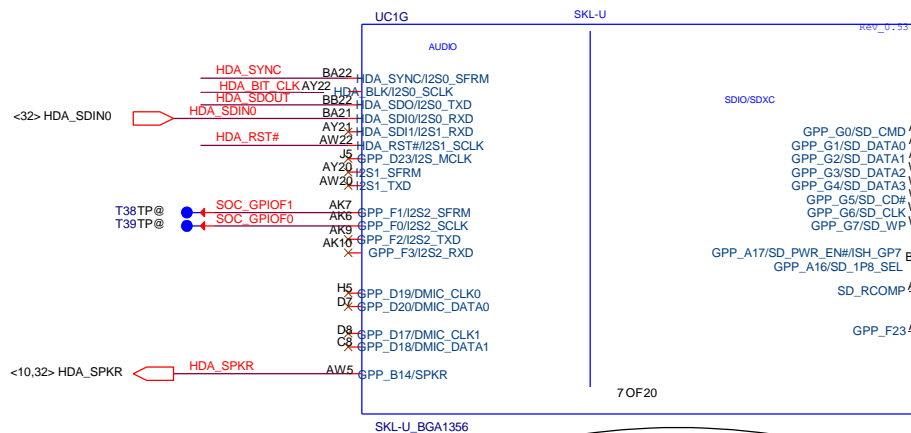
EON SA000046400 S IC FL 64M XN25Q64-104HIP SOP 8P MXIC
SA000046400 S IC FL 64M XN25Q64-104HIP SOP 8P MXIC
WINBOND SA000039A30 S IC FL 64M XN25Q64-104HIP SOP 8P MXIC
Micron SA000051100 S IC FL 64M XN25Q64-104HIP SOP 8P MXIC

ENE Fixed Code Block Diagram

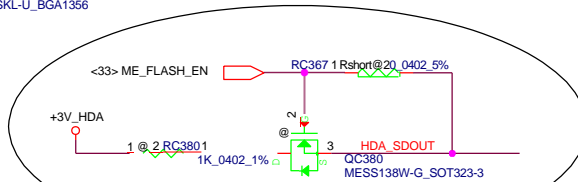
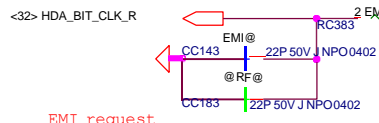
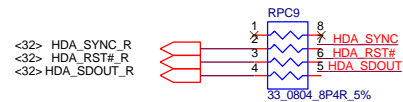


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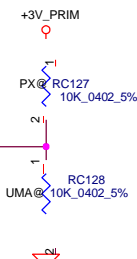
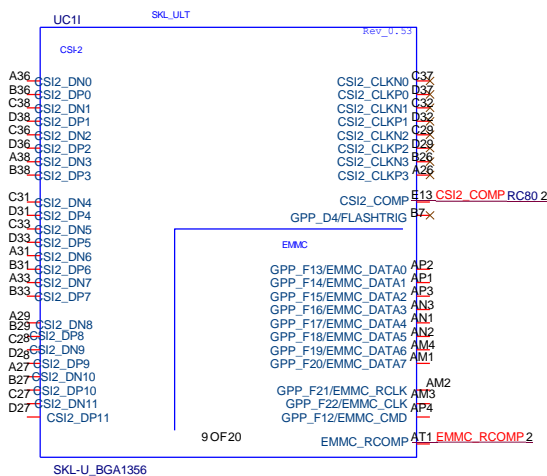
| | |
|-----------------------------|--------------------------|
| Compal Electronics, Inc. | |
| SKL-U(3/12)SPI,ESPI,SMB,LPC | |
| Document Number | EPK50_LA-G07CP |
| Date | Friday, January 05, 2018 |
| Sheet | 7 of 59 |



HDA for AUDIO



HDA_SDOUT:
ME Flash Descriptor Security Override
Low : Disabled(Default)
High : Enabled

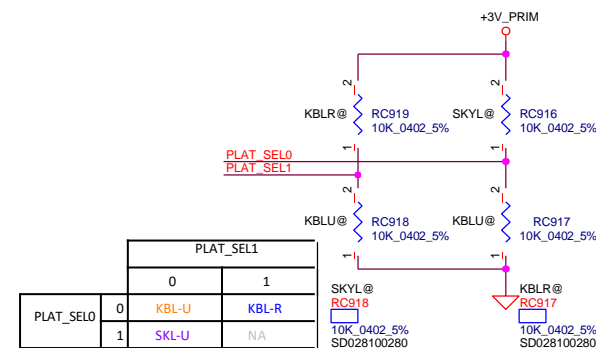
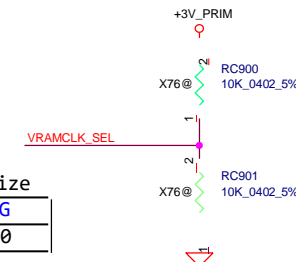


X76 BOM control RAM size

| Net Name | 4G | 2G |
|-------------|----|----|
| VRAMCLK_SEL | 1 | 0 |

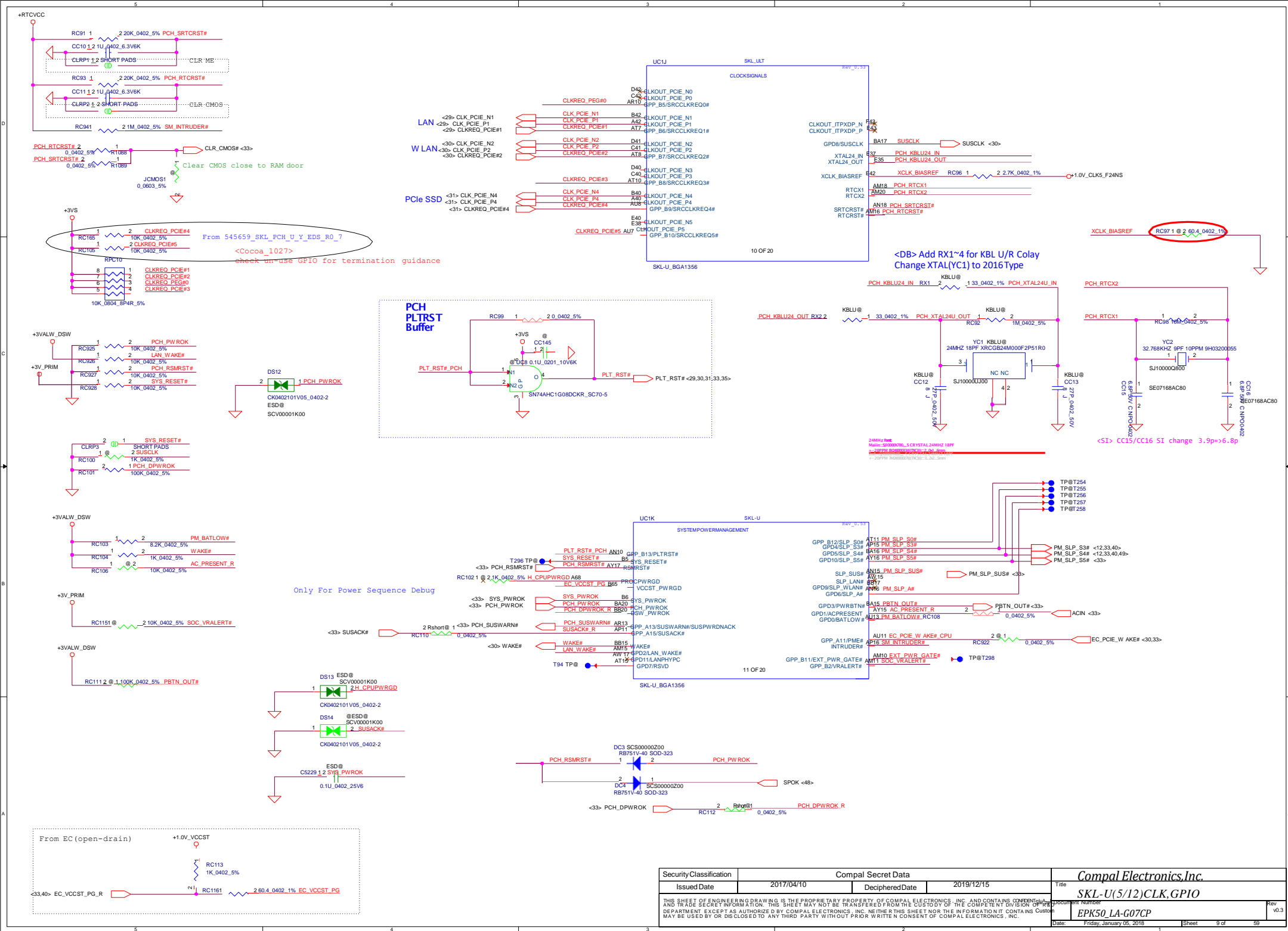
| | UMA | DIS |
|------------|-----|-----|
| PROJECT_ID | 0 | 1 |

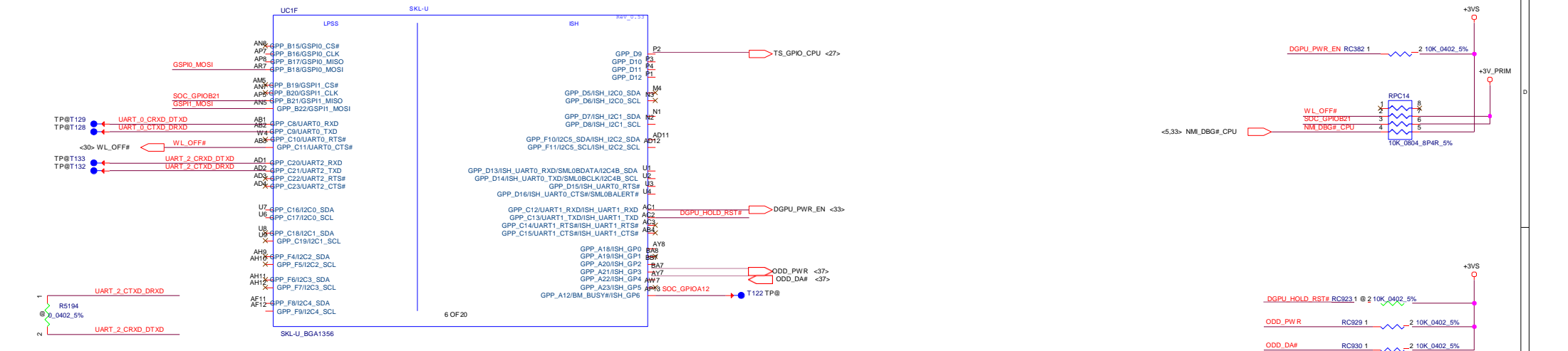
| | 2G VRAM | 4G VRAM |
|------------|---------|---------|
| VRAM Clock | 0 | 1 |



| | | PLAT_SEL1 | |
|-----------|---|-----------|-------|
| | | 0 | 1 |
| PLAT_SELO | 0 | KBL-U | KBL-R |
| | 1 | SKL-U | NA |

| | | | | |
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| | | | | Document Number |
| | | | | EPK50_LA-G07CP |
| | | | | Rev |
| | | | | v0.3 |
| | | | | Date |
| | | | | Friday, January 05, 2018 |
| | | | | Sheet |
| | | | | 8 of 59 |

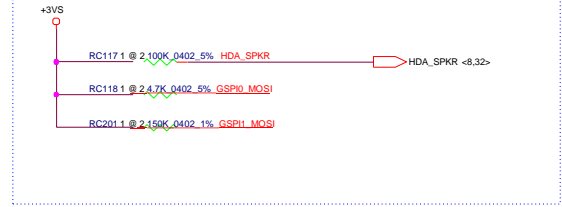




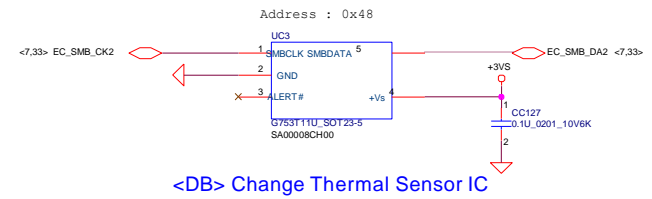
Functional Strap Definitions

- SPKR (Internal Pull Down):**
- TOP Swap Override
 - 0 = Disable TOP Swap mode.----> AAX05 Use
 - 1 = Enable TOP Swap Mode.
- GSPi0_MOSI (Internal Pull Down):**
- No Reboot
 - 0 = Disable No Reboot mode. --> AAX05 Use
 - 1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
- GSPi1_MOSI (Internal Pull Down):**
- Boot BIOS Strap Bit
 - 0 = SPI Mode --> AAX05 Use
 - 1 = LPC Mode

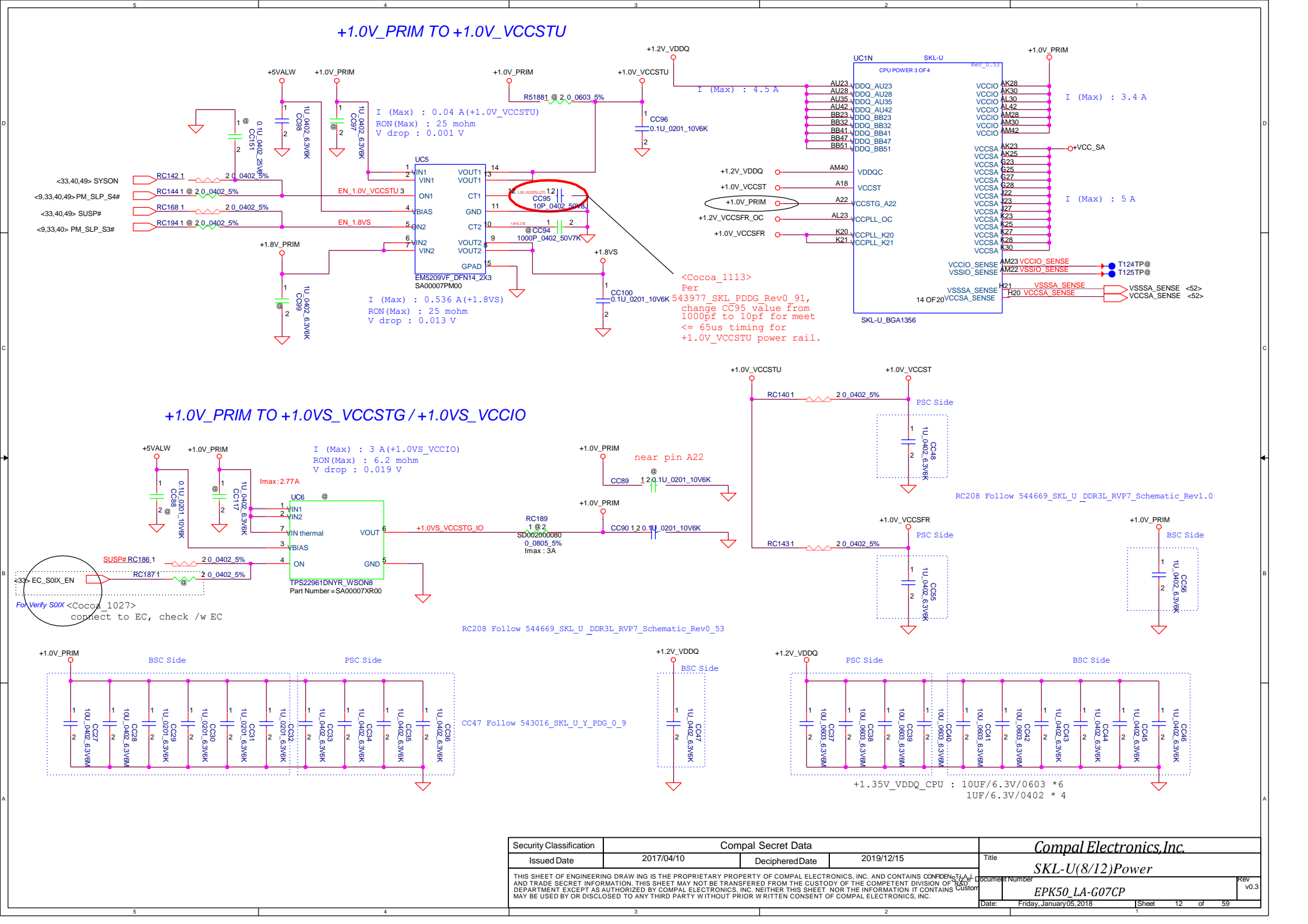
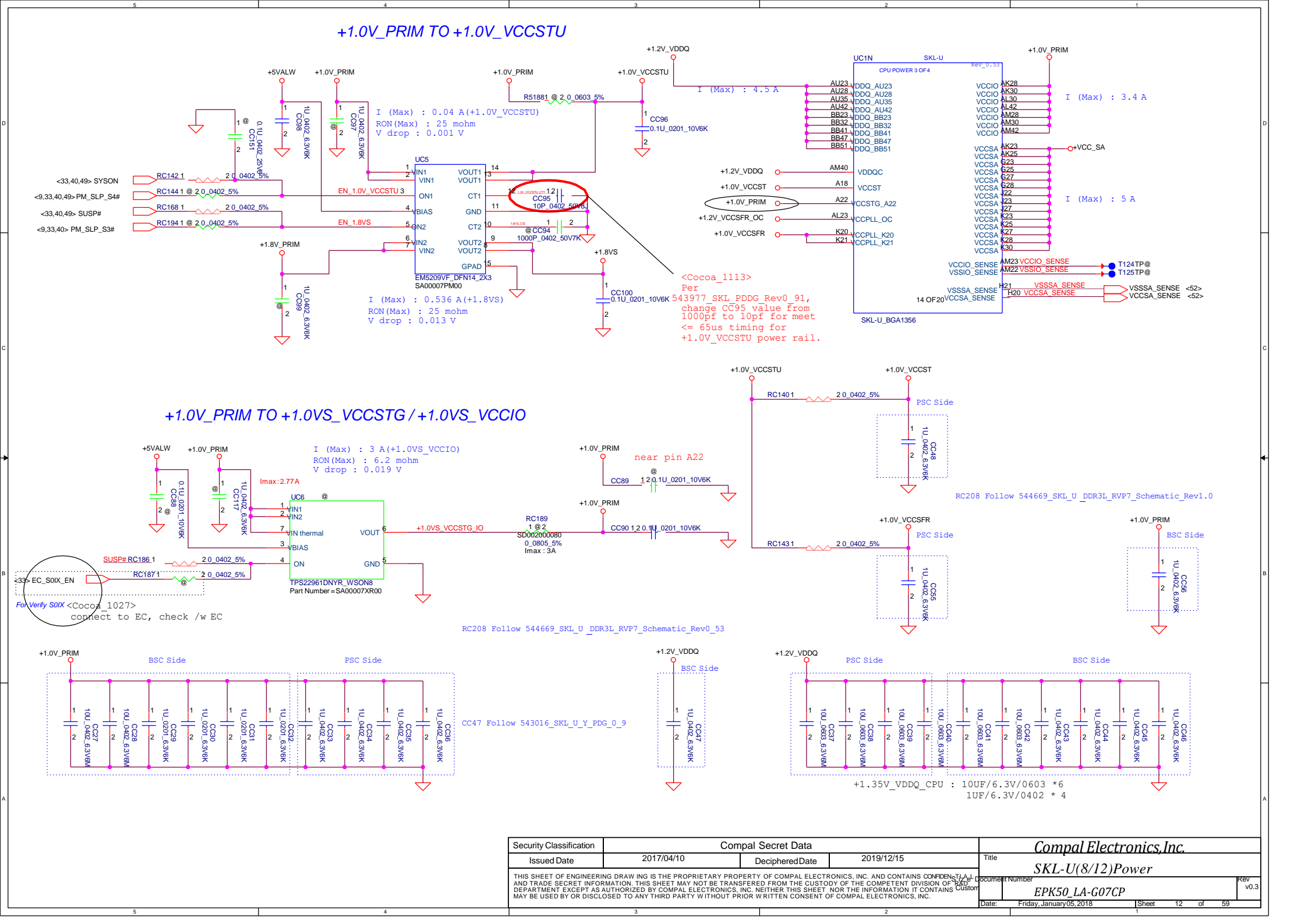
Strap Pin



CPU THERMAL SENSOR



| | | | | | |
|---|--------------------|-----------------|------------|--------------------------|----------------|
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| Date | | | | Friday, January 05, 2018 | Sheet 10 of 99 |



+1.0V_PRIM TO +1.0V_VCCSTU

+1.0V_PRIM TO +1.0VS_VCCSTG/+1.0VS_VCCIO

+1.2V_VDDQ

+1.35V_VDDQ_CPU

Security Classification
Compal Secret Data

Issued Date
2017/04/10

Deciphered Date
2019/12/15

Title
SKL-U(8/12)Power

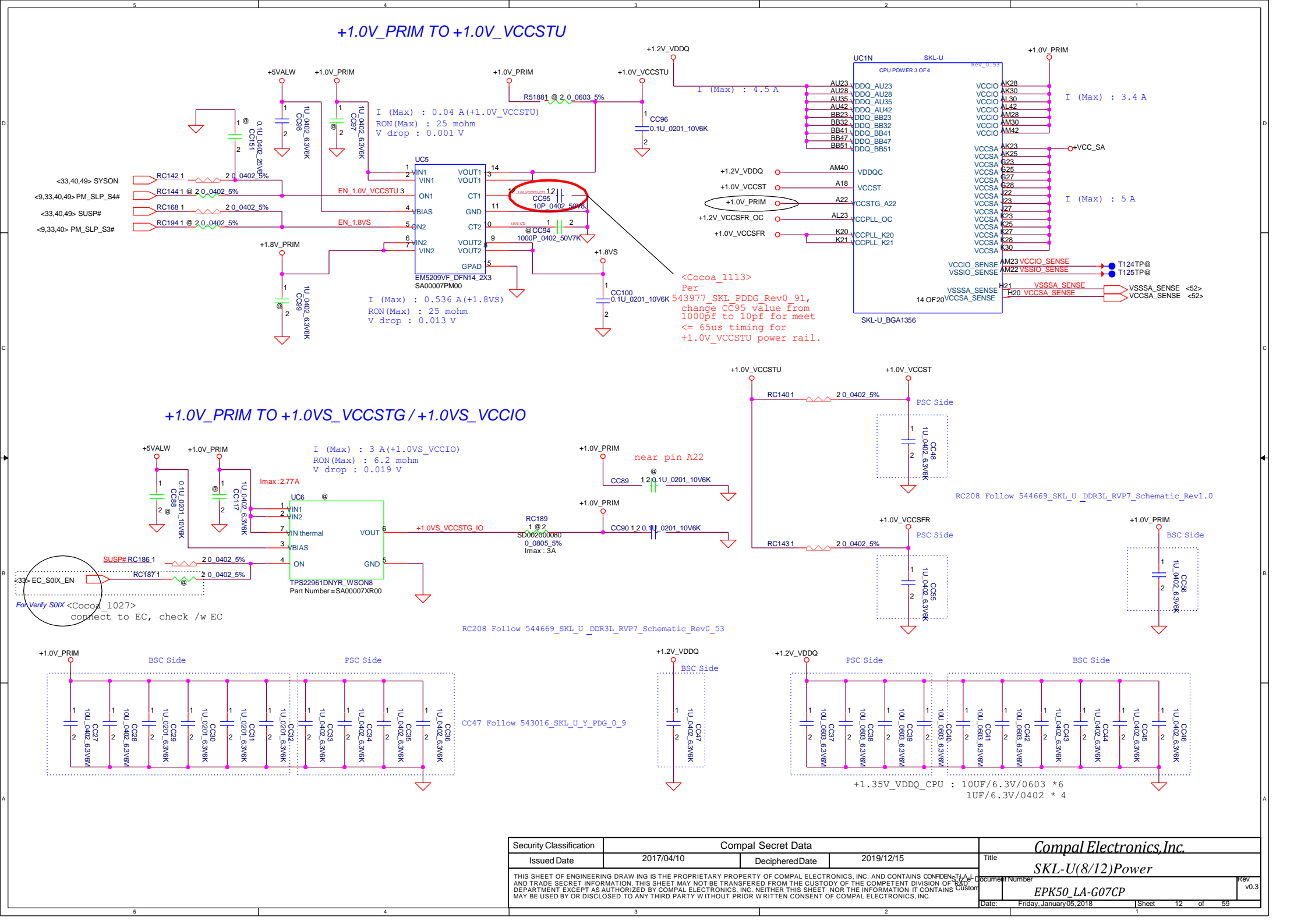
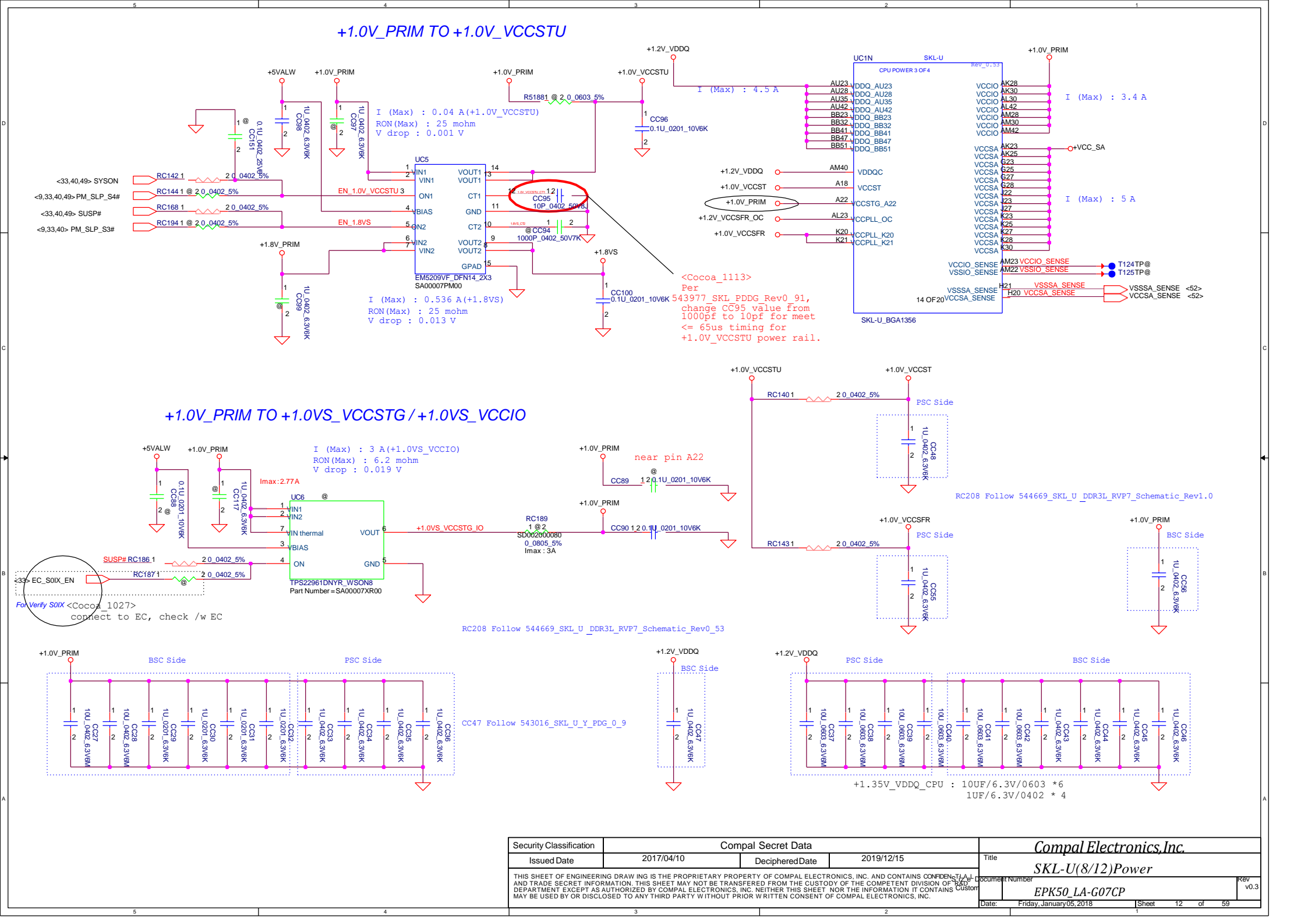
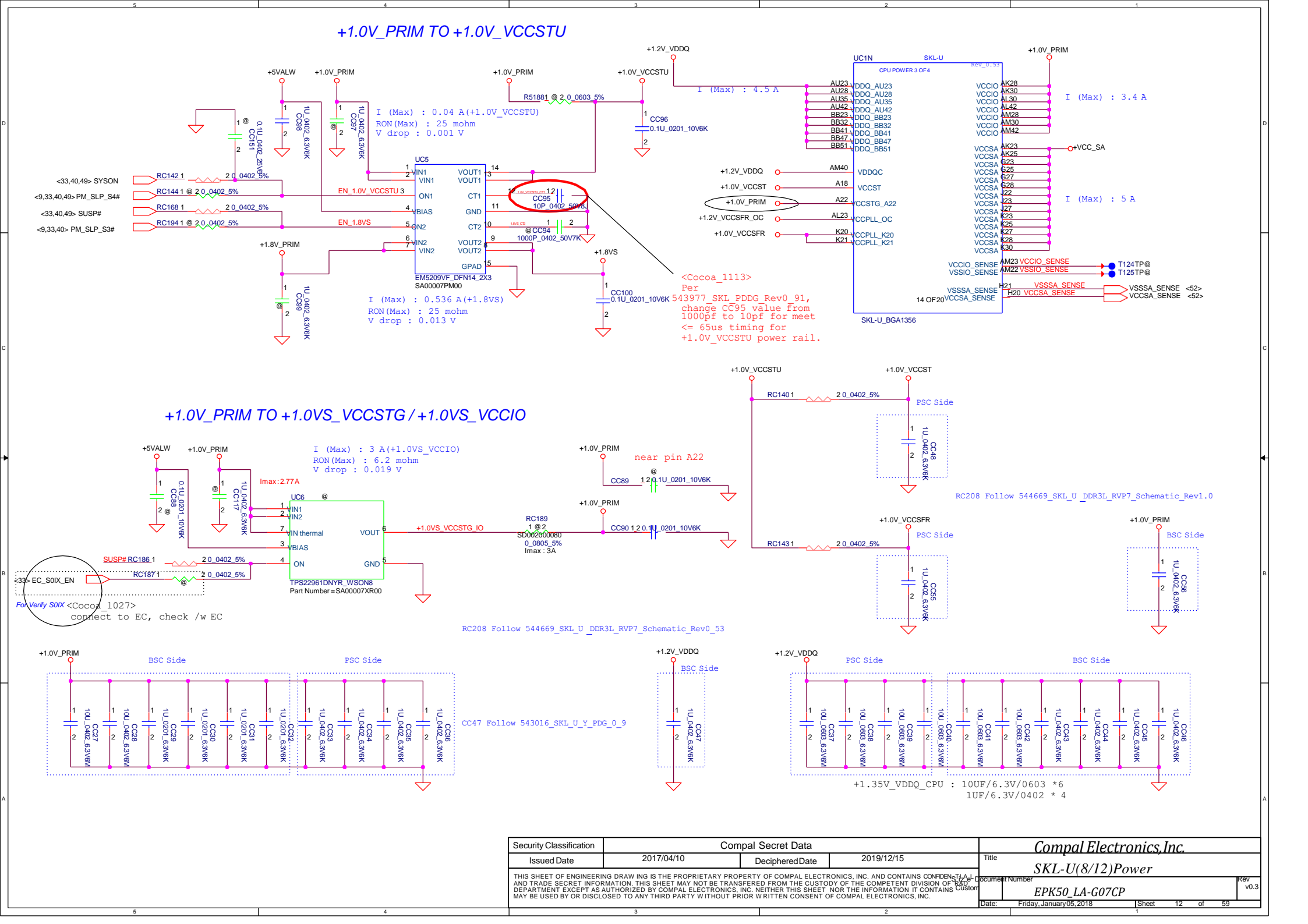
Document Number
EPK50_LA-G07CP

Date
Friday, January 05, 2018

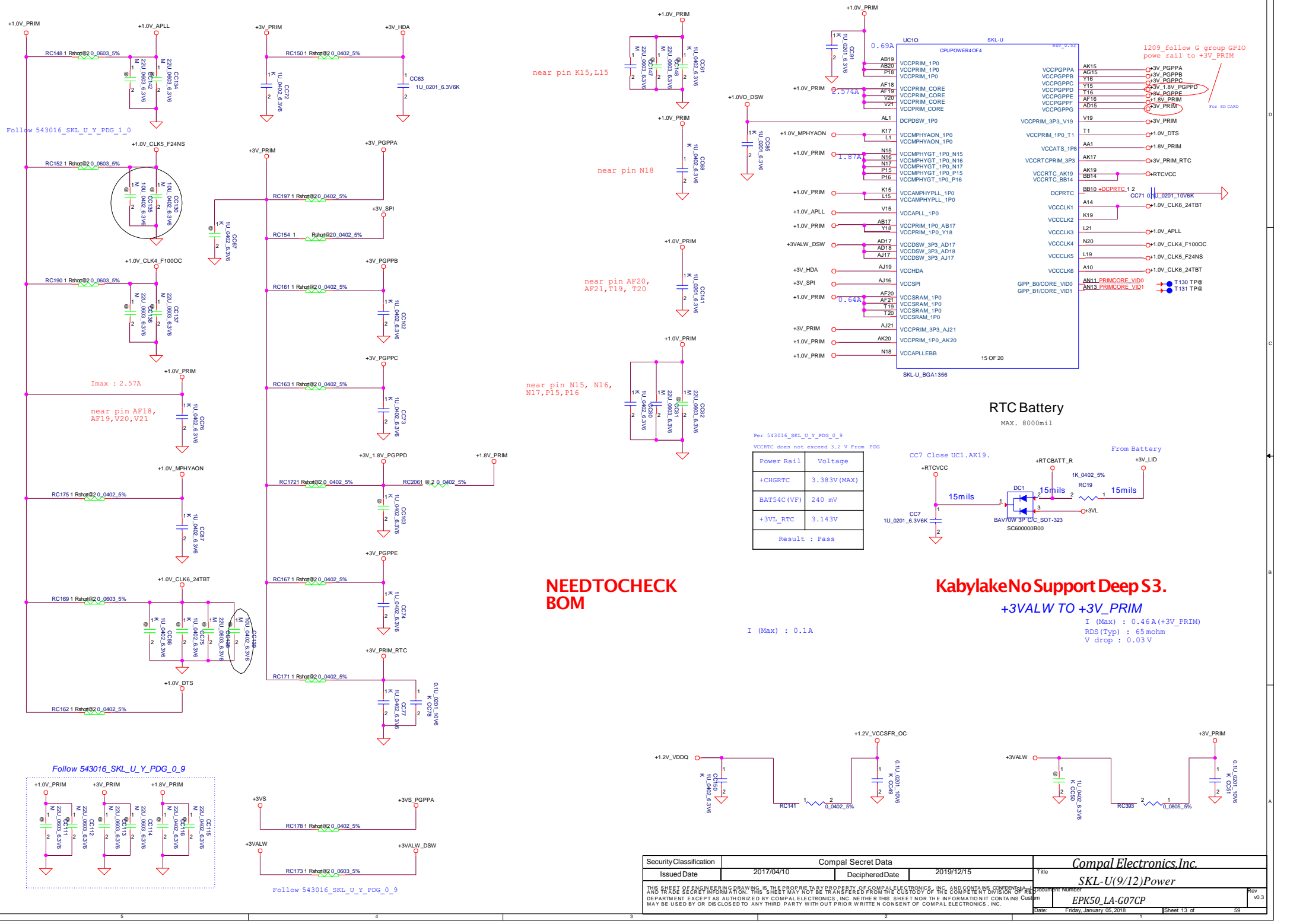
Sheet
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Rev
v0.3

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[illegible]

+1.0V_PRIM TO +1.0V_VCCSTU



near pin K15,L15

near pin N18

near pin AF20, AF21,T19, T20

near pin N15, N16, N17,P15,P16

NEEDTOCHECK BOM

Per 543016_SKL_U_Y_PDG_0_9

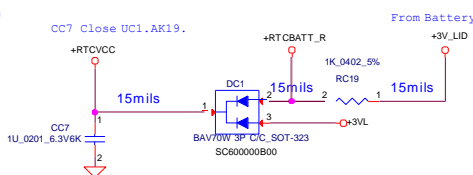
VCCRTC does not exceed 3.2 V from PDG

| Power Rail | Voltage |
|-------------|--------------|
| +CHGRTC | 3.383V (MAX) |
| BAT54C (VF) | 240 mV |
| +3VL_RTC | 3.143V |

Result : Pass

RTC Battery

MAX. 8000mil



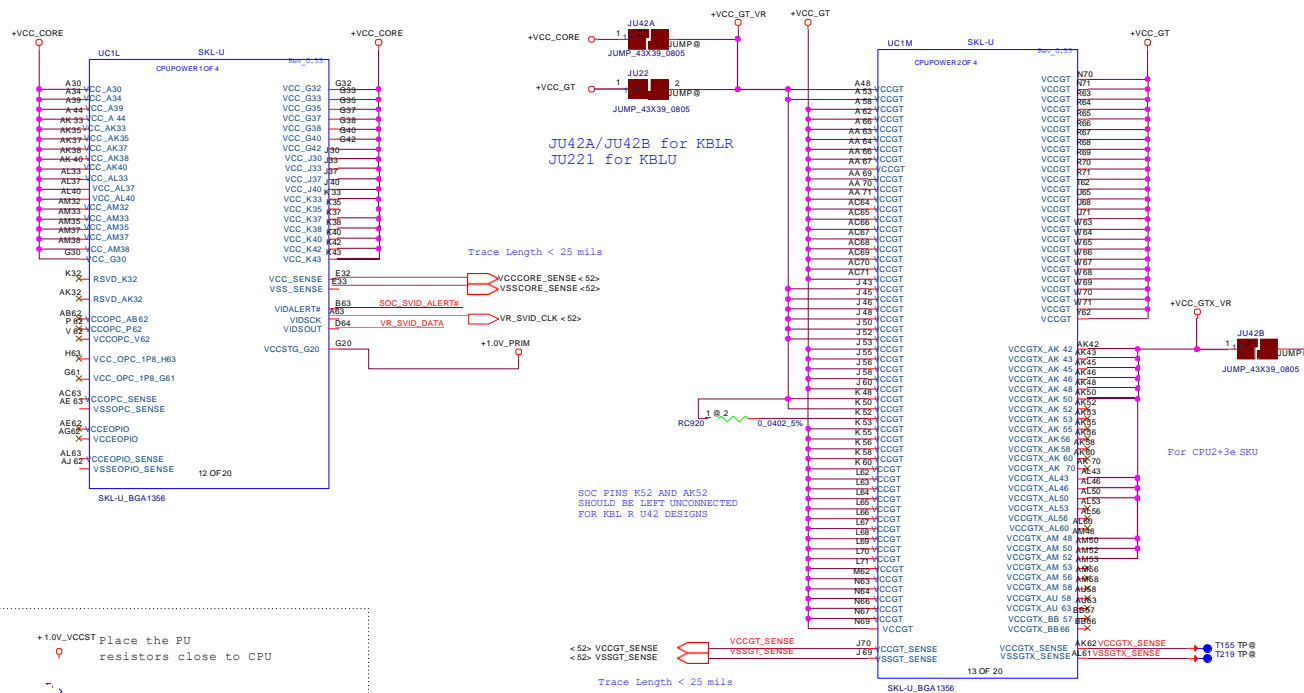
KabyLakeNo Support Deep S3.

+3VALW TO +3V_PRIM

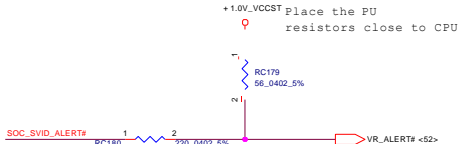
I (Max) : 0.46 A (+3V_PRIM)
RDS (Typ) : 65mohm
V drop : 0.03 V

| | | | | | |
|---|------------|--------------------|------------|--------------------------------|----------------|
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| Issued Date | 2017/04/10 | Deciphered Date | 2019/12/15 | SKL-U(9/12)Power | |
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| | | | | Date: Friday, January 05, 2018 | Sheet 13 of 59 |

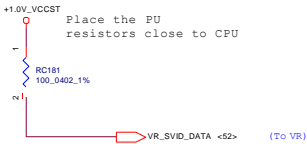
For CPU2+3e SKU



SVID ALERT

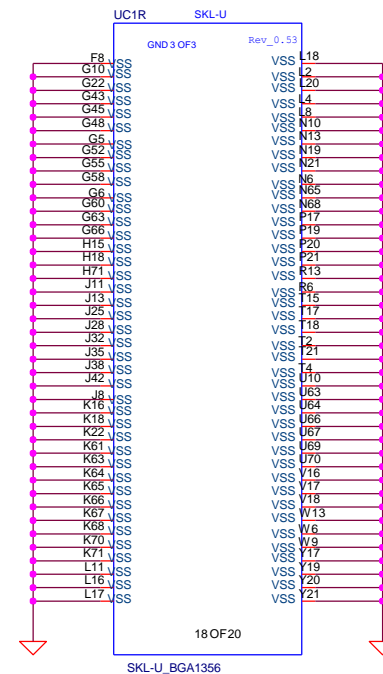
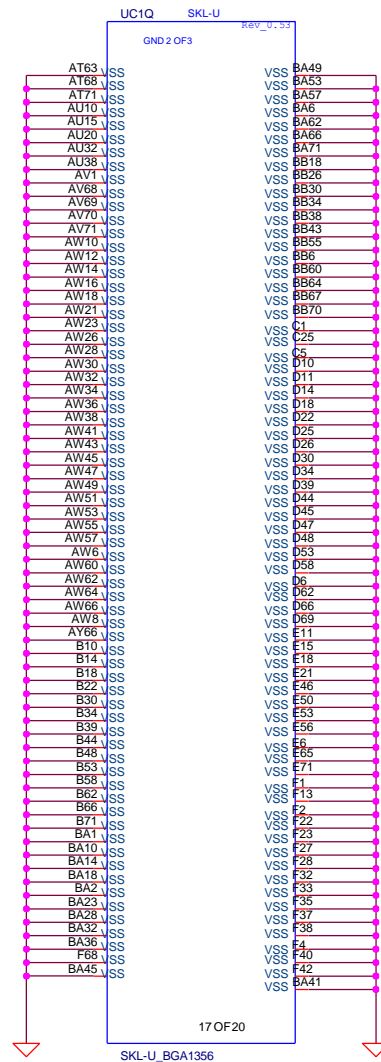
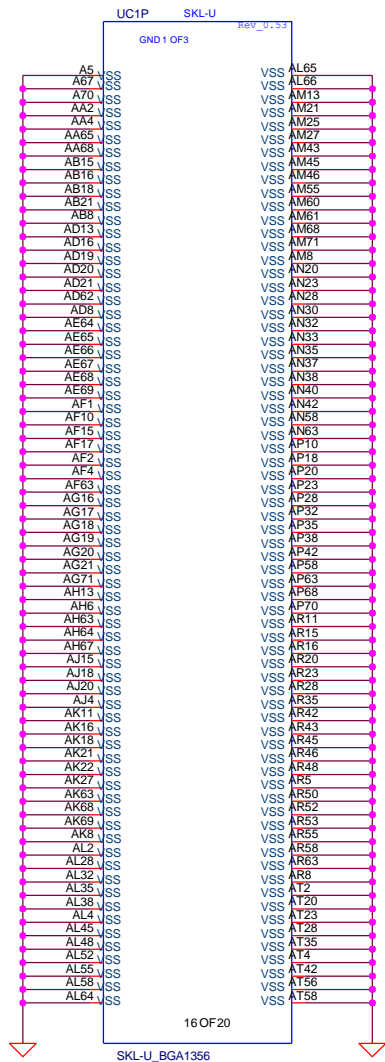


SVID DATA



| Ball # | Ball Names R-U42 | Ball Names U22 | R-U42/U22 common board guidelines |
|--------|------------------|----------------|--|
| C7 | XTAL24_OUT | NC | connect to R-U42 XTAL24_OUT |
| E3 | XTAL24_IN | NC | connect to R-U42 XTAL24_IN |
| E35 | NC | XTAL24_OUT | connect to U22 XTAL24_OUT |
| E37 | NC | XTAL24_IN | connect to U22 XTAL24_IN |
| AK42 | VCCCORE | VccGTx | connect to VccGTx/VCCCORE power plane island |
| AK43 | VCCCORE | VccGTx | |
| AK45 | VCCCORE | VccGTx | |
| AK46 | VCCCORE | VccGTx | |
| AK48 | VCCCORE | VccGTx | |
| AK50 | VCCCORE | VccGTx | |
| AL43 | VCCCORE | VccGTx | |
| AL46 | VCCCORE | VccGTx | |
| AL50 | VCCCORE | VccGTx | |
| AM48 | VCCCORE | VccGTx | |
| AM50 | VCCCORE | VccGTx | connect to VccGT/VCCCORE power plane island |
| AM52 | VCCCORE | VccGTx | |
| J43 | VCCCORE | VCCGT | |
| J45 | VCCCORE | VCCGT | |
| J46 | VCCCORE | VCCGT | |
| J48 | VCCCORE | VCCGT | |
| J50 | VCCCORE | VCCGT | |
| J52 | VCCCORE | VCCGT | |
| K48 | VCCCORE | VCCGT | |
| K50 | VCCCORE | VCCGT | |
| A48 | VCCCORE | VCCGT | Must Not Be Connected. RVP use this signal for debug and testing purpose only. |
| A53 | VCCCORE | VccGTx | |
| AK52 | RSVD | VccGTx | |
| K52 | RSVD | VCCGT | Must Not Be Connected. RVP use this signal for debug and testing purpose only. |

| | | | | | |
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| Date | | | | Friday, January 05, 2018 | Sheet 14 of 59 |



| | | | | | | |
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| | | | | EPK50_LA-G07CP | v0.3 | |
| Date: Friday, January 05, 2018 | | | | Sheet | 15 | of 59 |

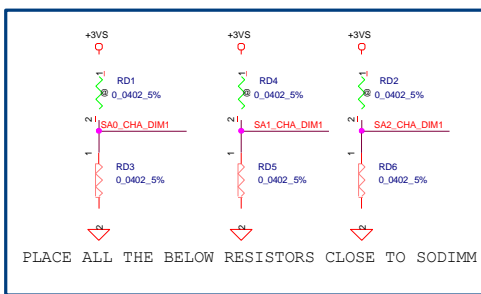
SI 1/15SI 1/15

CHANNEL-A

REVERSE TYPE

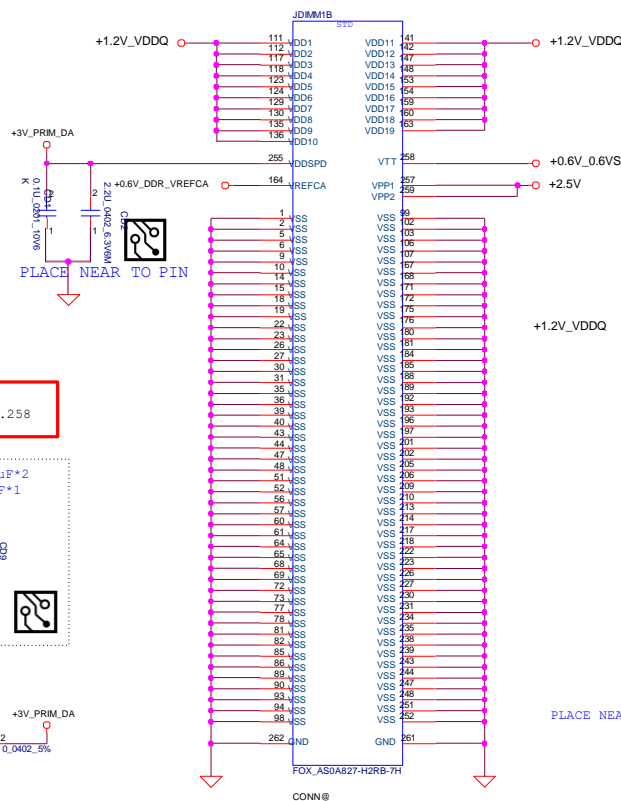
Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM

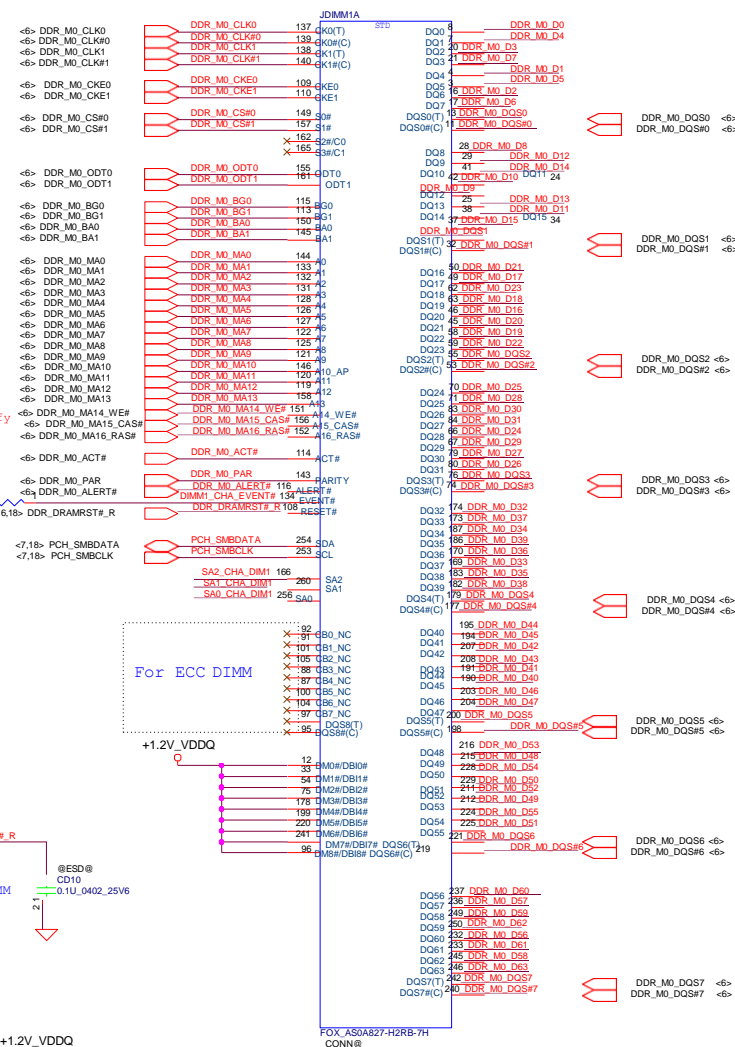


SPD ADDRESS FOR CHANNEL A :
 WRITE ADDRESS: 0XA0
 READ ADDRESS: 0XA1
 SA0 = 0; SA1 = 0; SA2 = 0.
 DDR4 POR OPERATING SPEED: 1867 MT/S
 STRETCH GOAL IS 2133 MT/S

<6> DDR_M0_D[0..15]
 <6> DDR_M0_D[16..31]
 <6> DDR_M0_D[32..47]
 <6> DDR_M0_D[48..63]

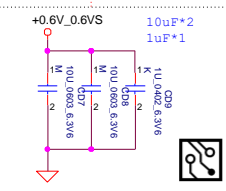
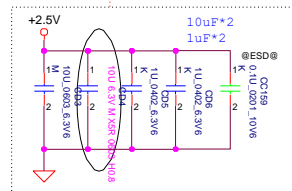


Part Number: LTCX0069GA0
 Part Value: S SOCKET FOX AS0A827-H2RB-7H 260P DDR4

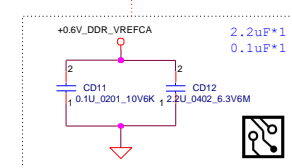


Layout Note:
 Place near JDIMM1.257,259

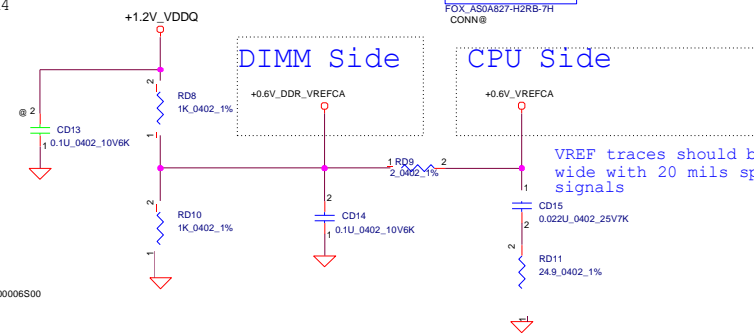
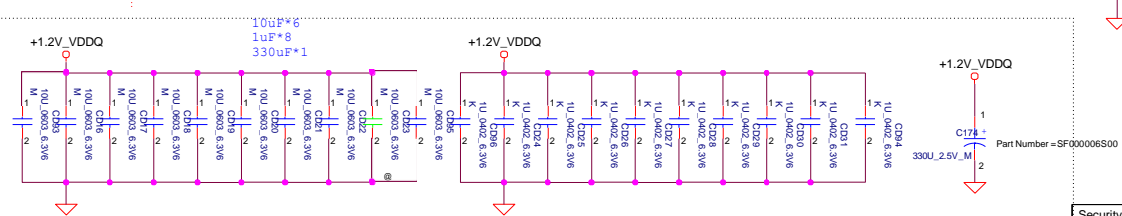
Layout Note:
 Place near JDIMM1.258



Layout Note:
 PLACE THE CAP near JDIMM1. 164



Layout Note:
 Place near JDIMM1

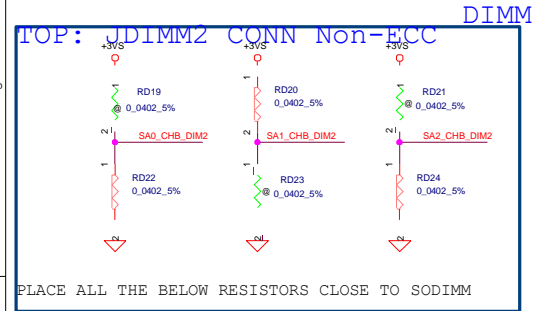


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| | | | | | | Date | Friday, January 05, 2018 | Sheet 17 of 59 |

CHANNEL-B

Interleaved Memory

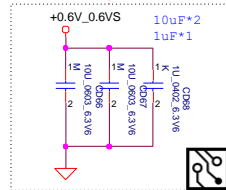
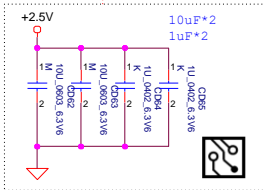
STD (5.2 mm)



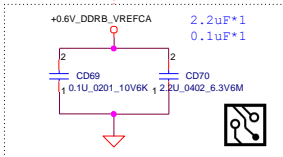
SPD ADDRESS FOR CHANNEL B :
 WRITE ADDRESS: 0XA4
 READ ADDRESS: 0XA3
 SA0 = 0; SA1 = 1; SA2 = 0.
 DDR4 POR OPERATING SPEED: 1867 MT/S
 STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259

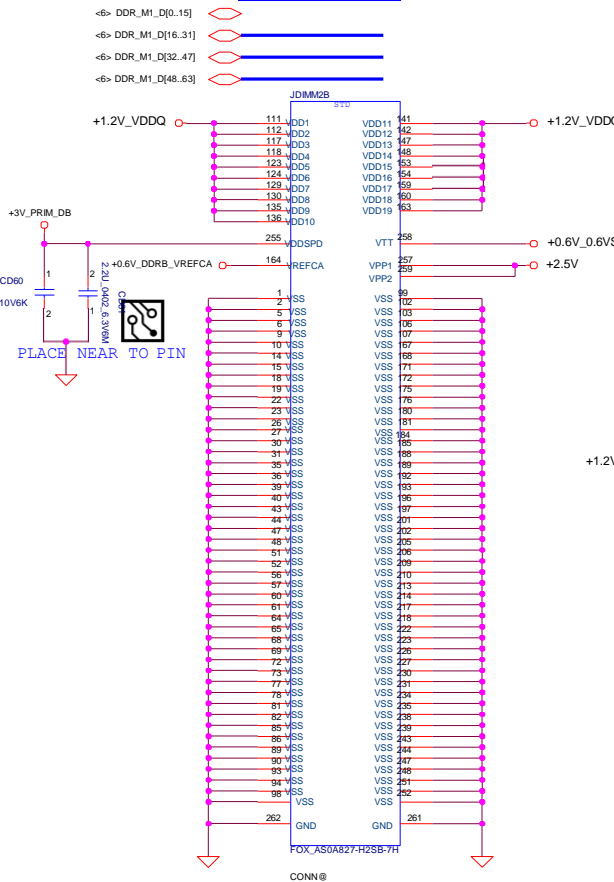
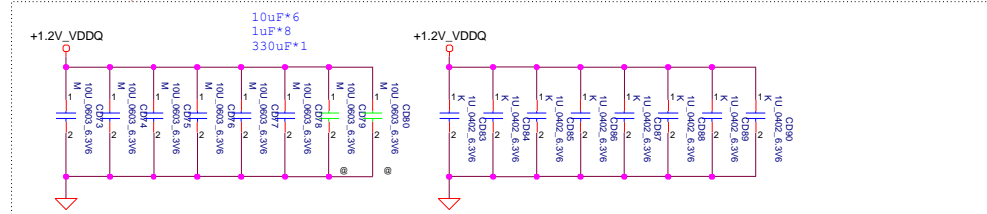
Layout Note:
Place near JDIMM2.258



Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2

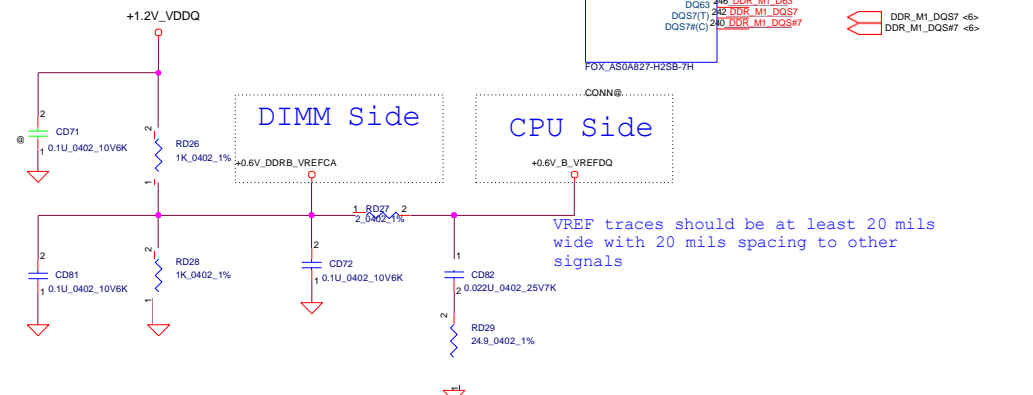


Layout Note:
Place near JDIMM2



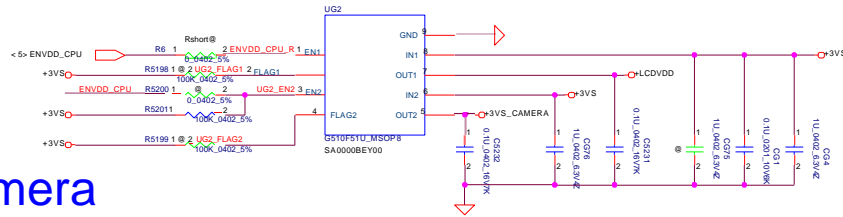
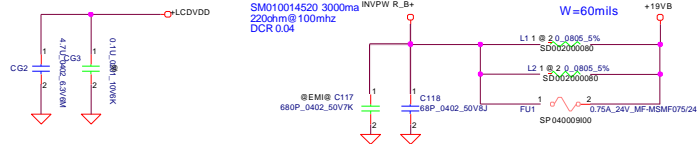
Part Number: LTCX0069FA0
 Part Value: S SOCKET FOX AS0A827-H2SB-7H 260P DDR4

Part Value: S SOCKET FOX AS0A827-H2SB-7H 260P DDR4

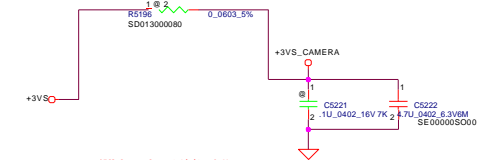
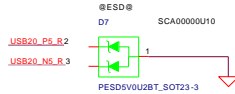
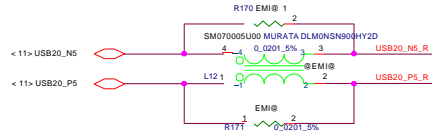


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| Friday, January 05, 2018 | | | | Date | Rev v0.3 | |
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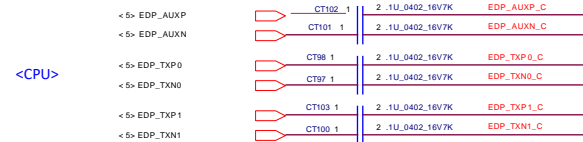
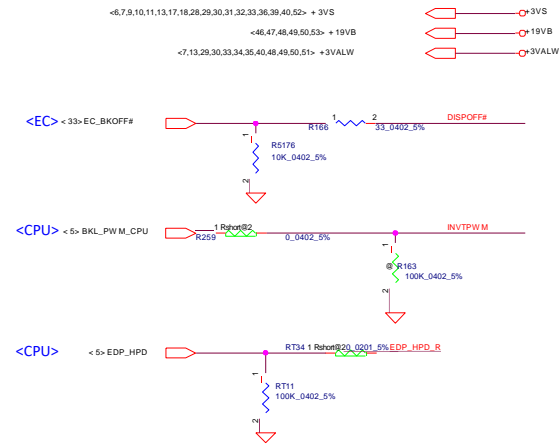
DP Power



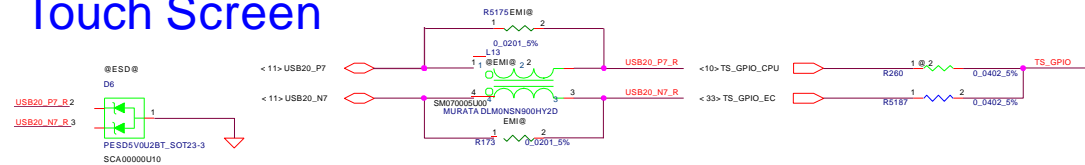
Camera



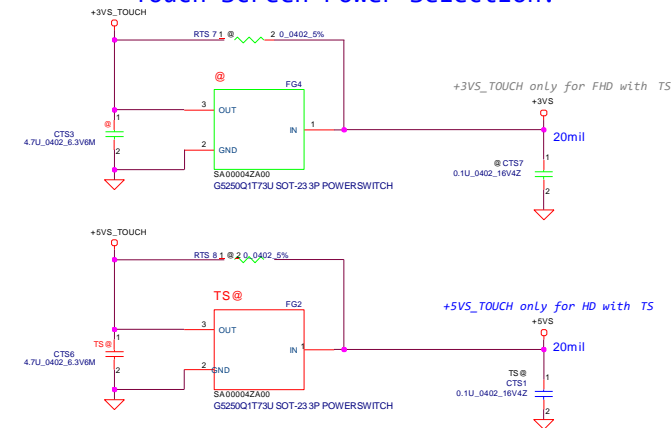
*FG3 Camera Current Limit : 0.4A
1st:S4000080300, S IC G5250Q173U SOT-23 3P POWER SWITCH_0.4A
2nd:S4000042A00, S IC AP2330W-7 SC59 3P PWR SW_0.4A



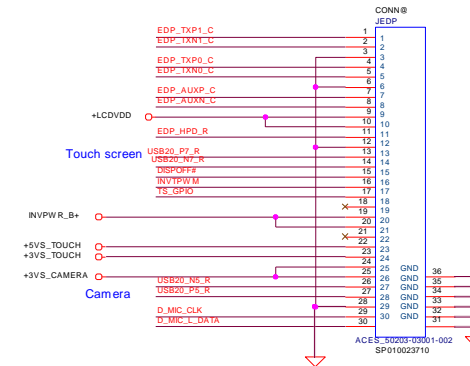
Touch Screen



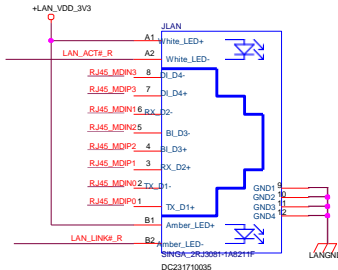
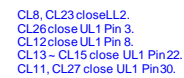
Touch Screen Power Selection:

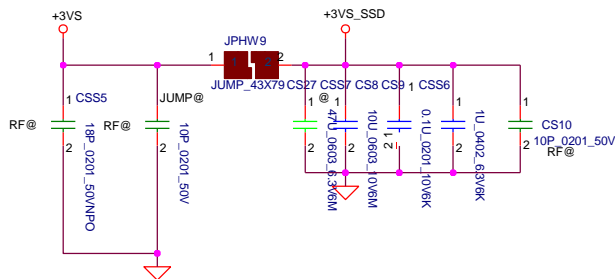


eDP



| | | | | | | | | |
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| | | | | Date: Friday, August 05, 2016 | | Sheet 27 of | | 59 |





<6,7,9,10,11,13,17,18,27,28,29,30,32,33,36,39,40,52>

+3VS

+3VS

Figure 12-1. PCI Express® Link Configurations Supported by the Guidelines in this Chapter

| PCH-LP Details | PCIe® Controller #1 | | | | PCIe® Controller #2 | | | | PCIe® Controller #3 | | | |
|-----------------|---------------------|------|------|------|---------------------|------|------|------|---------------------|-------|-------|-------|
| Flex I/O Lane # | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| PCIe® Lane # | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| Base-U | 1x4 | RP 1 | | | RP 5 | | | | RP 9 | | | |
| | 1x4 LR | RP 1 | | | RP 5 | | | | RP 9 | | | |
| | 2x2 | RP 1 | RP 3 | RP 3 | RP 5 | | | | RP 9 | RP 11 | RP 11 | RP 12 |
| | 1x2+2x1 | RP 1 | RP 3 | RP 4 | RP 5 | | | | RP 9 | RP 11 | RP 11 | RP 12 |
| | 2x1+1x2 | RP 4 | RP 3 | RP 1 | RP 5 | | | | RP 12 | RP 11 | RP 9 | |
| Premium-U | 4x1 | RP 1 | RP 2 | RP 3 | RP 4 | RP 5 | RP 6 | RP 7 | RP 8 | RP 9 | RP 10 | RP 11 |
| | 1x4 | RP 1 | | | RP 5 | | | | RP 9 | | | |
| | 1x4 LR | RP 1 | | | RP 5 | | | | RP 9 | | | |
| | 2x2 | RP 1 | RP 3 | RP 3 | RP 5 | RP 7 | RP 8 | | RP 9 | RP 11 | RP 11 | RP 12 |
| | 1x2+2x1 | RP 1 | RP 3 | RP 4 | RP 5 | RP 7 | RP 8 | | RP 9 | RP 11 | RP 11 | RP 12 |

<SSD>

<11> PCIE_CRX_DTX_N11
<11> PCIE_CRX_DTX_P11

<11> PCIE_CTX_C_DRX_N11
<11> PCIE_CTX_C_DRX_P11

<11> PCIE_CRX_DTX_P12
<11> PCIE_CRX_DTX_N12

<11> PCIE_CTX_C_DRX_N12
<11> PCIE_CTX_C_DRX_P12

<9> CLK_PCIE_N4
<9> CLK_PCIE_P4

SSD1_IF PU on CPU side RPC13.3-10K
@ RS21
100K_0402_5%

<11> SSD1_IF

+3VS
@EMI @ CS16
VARIST_CK0402101V050402

SSD_PDET
+3VS
RS22 1 2
10K_0402_5%

Q51 SB000009Q80
2N7002KW_SOT323-3

pre PV: change to 10K for redriver detect pin voltage level

Key TYP.M

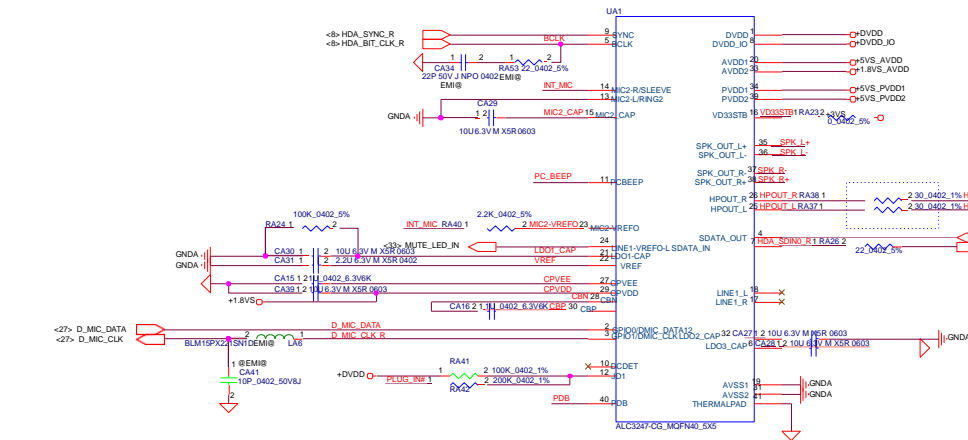
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|----|-------|---|----|---------|---------------------|----|-------|--------------------------------------|
| 39 | GND | PCIE_MVMe_D09000NU90_MZVLW1T0HMLH00H1_F73H1Q_09V1 | 39 | GND | Return Current Path | 40 | GND | Return Current Path |
| 41 | PETn0 | PCIe TX | 42 | N/C | | 43 | PETp0 | Transmitter Differential Signal Pair |
| 43 | PETp0 | PCIe TX | 44 | N/C | | 45 | PETn0 | Transmitter Differential Signal Pair |
| 45 | GND | Return current path | 46 | N/C | | 47 | PETp0 | Transmitter Differential Signal Pair |
| 47 | PERn0 | PCIe Rx | 48 | N/C | | 49 | PERp0 | Receiver Differential Signal Pair |
| 49 | PERp0 | PCIe Rx | 50 | PERST# | | 51 | GND | Return Current Path |
| 51 | GND | Return current path | 52 | CLKREQ# | | 52 | GND | Return Current Path |

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express® Multiplexed Ports

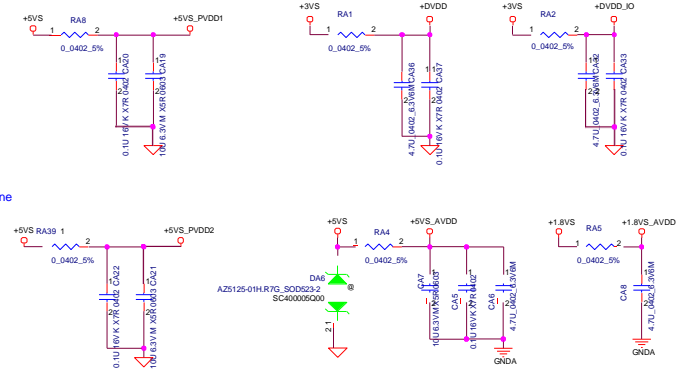
The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe® multiplexed ports.

Note: When SATA and PCIe® are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

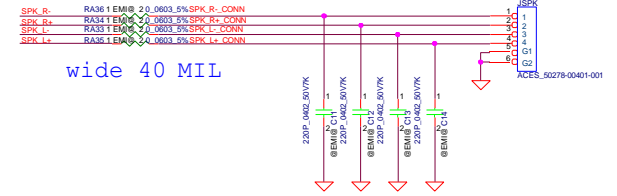
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| | | | | Date | Friday, January 05, 2018 |
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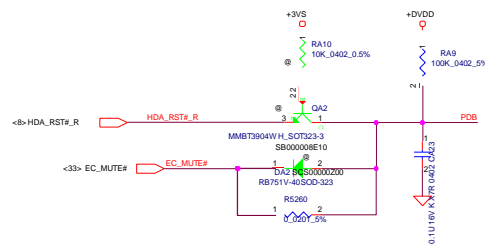
Headphone



Internal SPK



wide 40 MIL



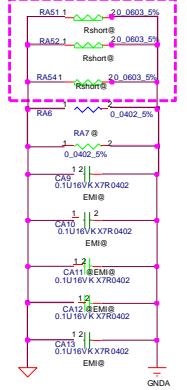
PC BEEP

EC BEEP<3> EC_BEEP#

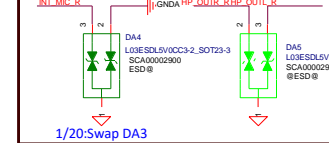
SB BEEP<8,10> HDA_SPKR

Close to Codec pin34

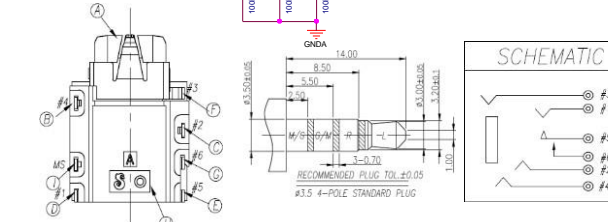
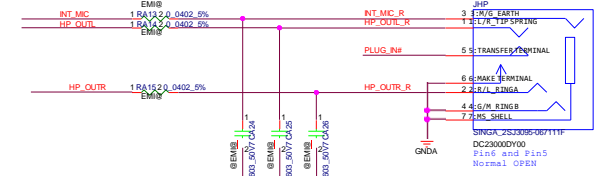
Place RAS1/RAS2/RAS3 on top of U1 RST side



Reserve for ESD request.

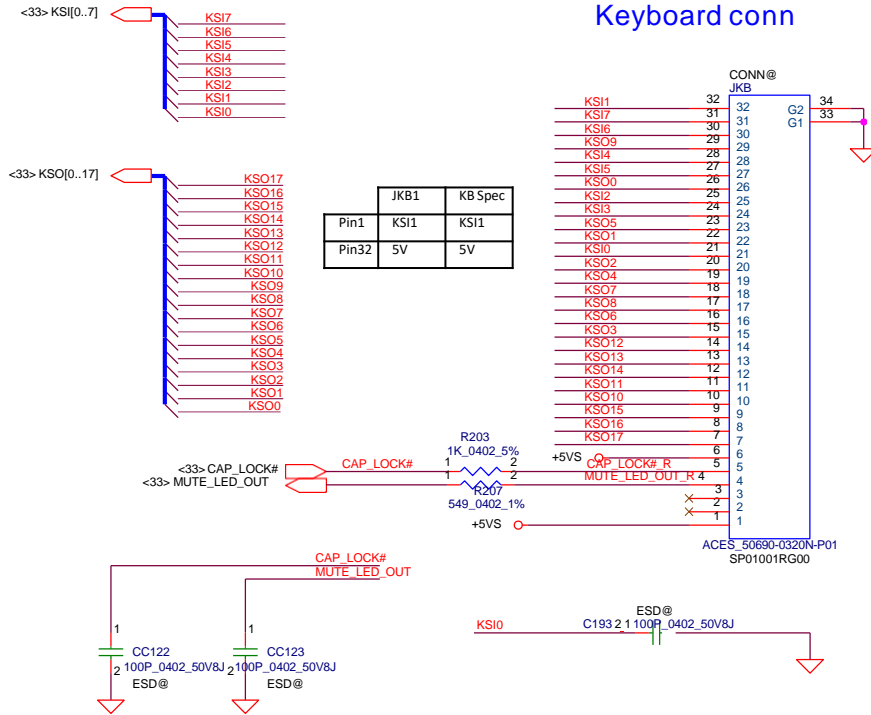
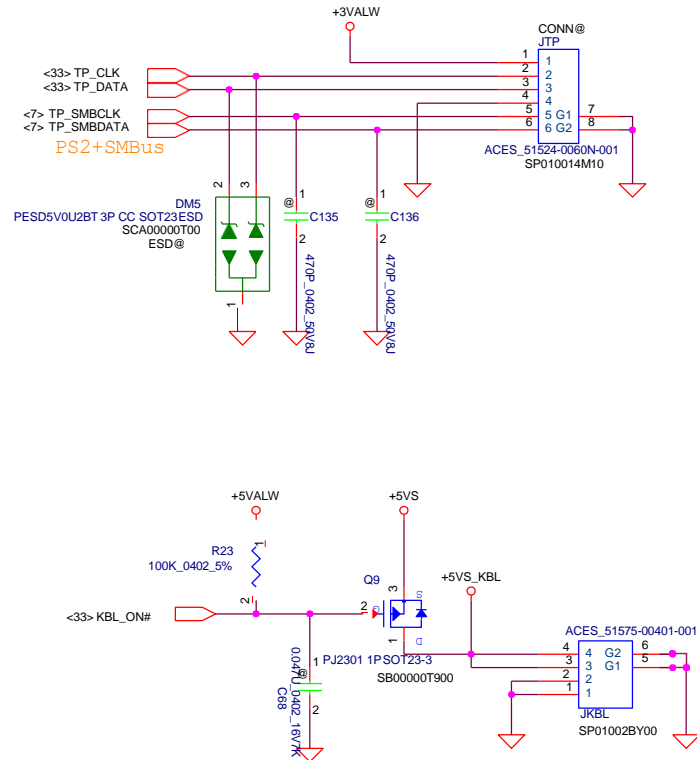


1/20 Swap DA3

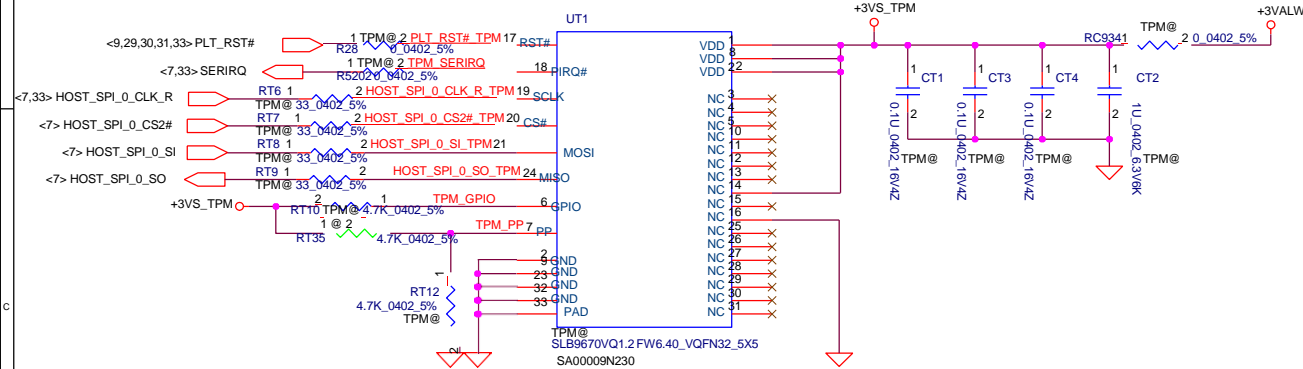


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| Date: Friday, January 05, 2018 | | | | Sheet 32 of 58 | |

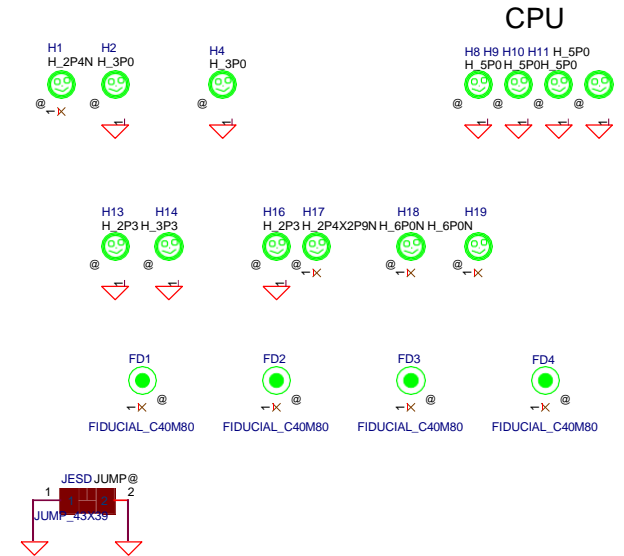
TP Button BD Connector



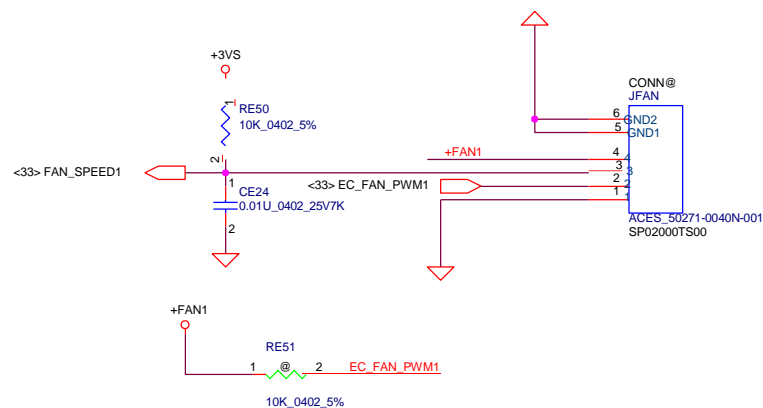
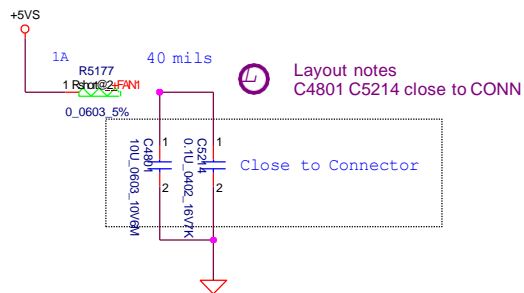
TPM2.0



Screw Hole



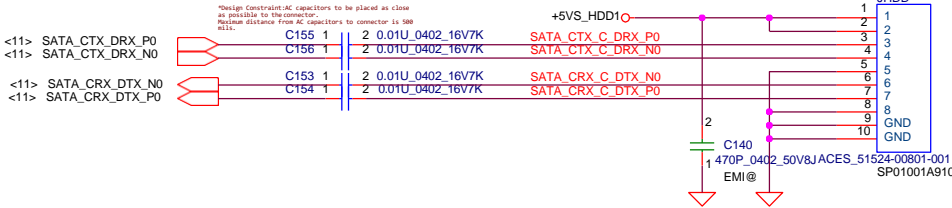
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|---|------------|--------------------|------------|--------------------------|--------------------------|
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| | | | | Sheet | 35 of 59 |
| | | | | Rev | v0.3 |



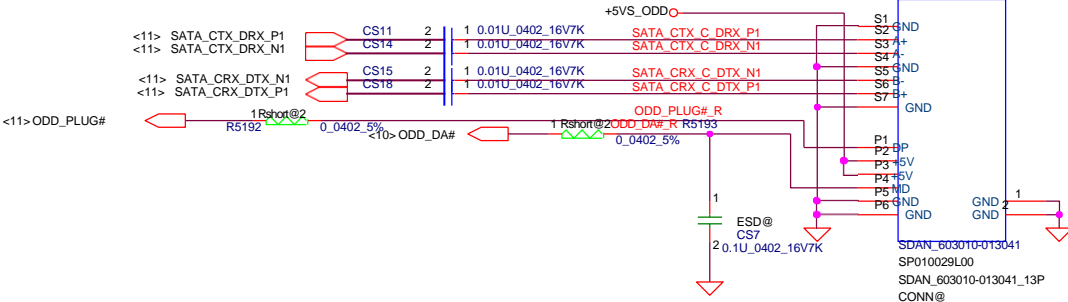
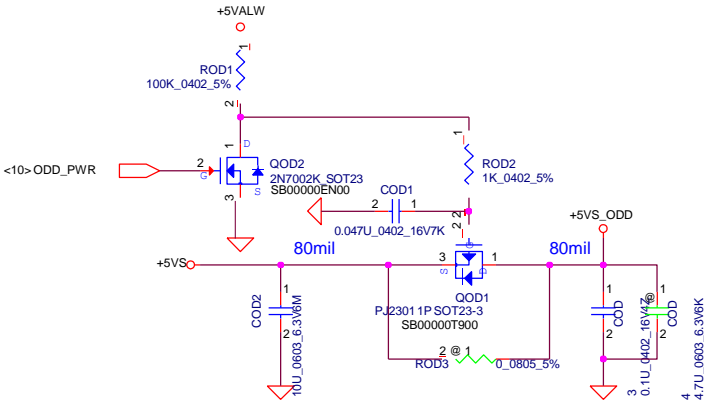
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| | | | | Date: Friday, January 05, 2018 | Sheet 36 of 59 |

2.5" SATA HDD

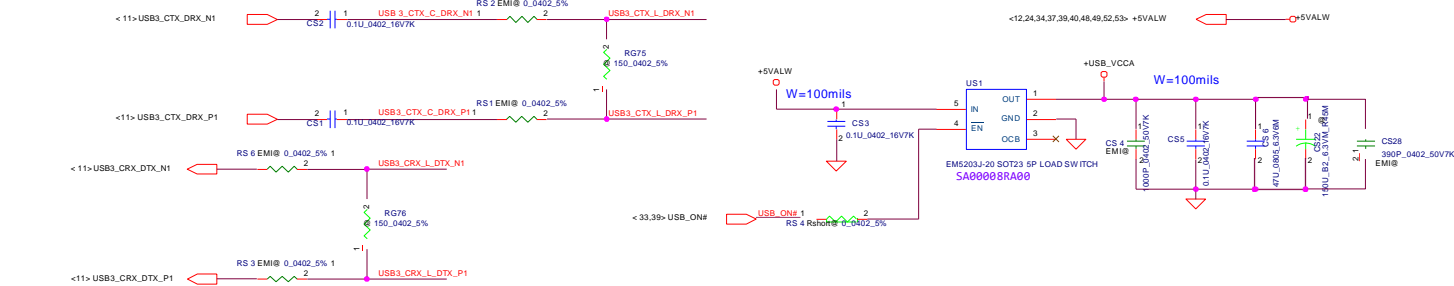
<PV> change short pad



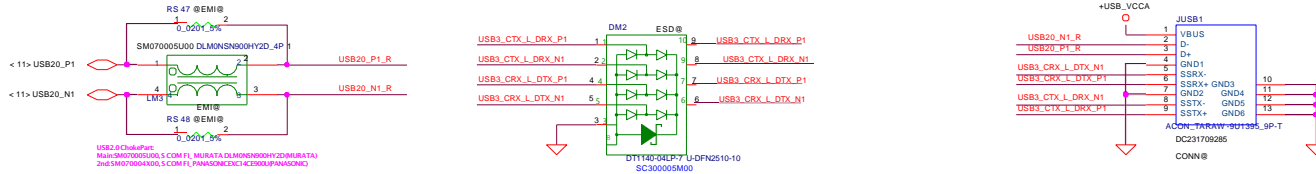
SATA ODD



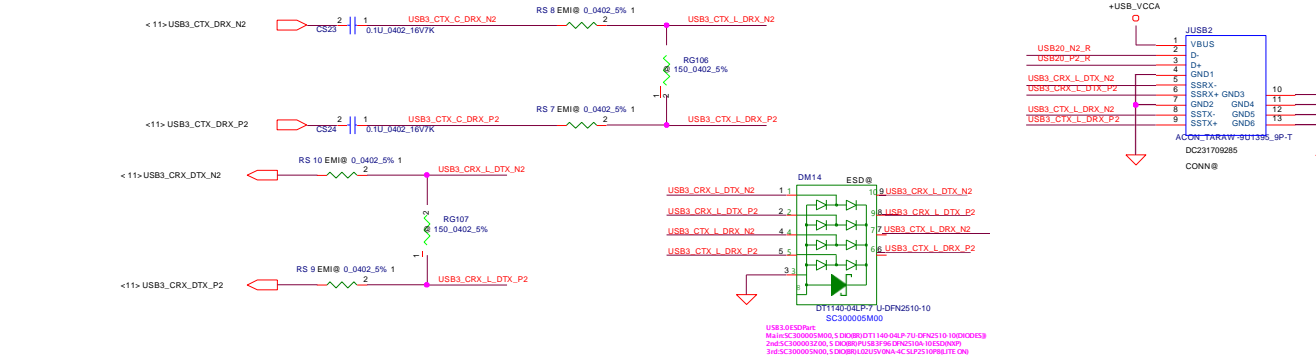
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| 2017/08/24 | | 2018/08/24 | | Title | |
| | | | | HDD/ODD Conn | |
| | | | | Document Number | |
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| | | | | Sheet | |
| | | | | 37 of 59 | |

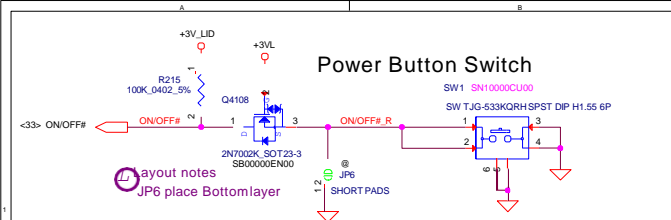


USB2.0/USB3.0 port 1

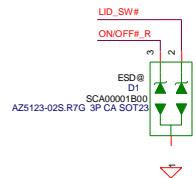


USB2.0/USB3.0 port 2

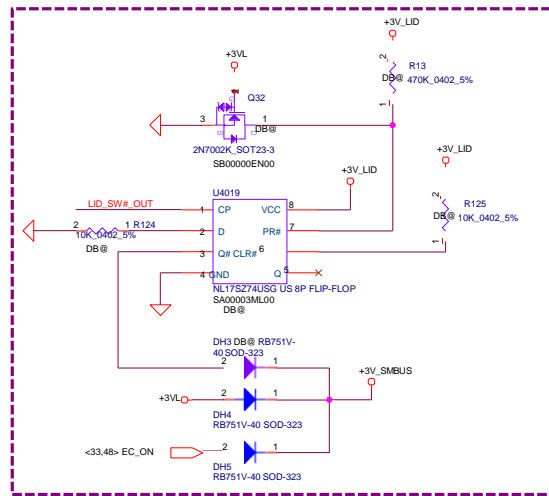
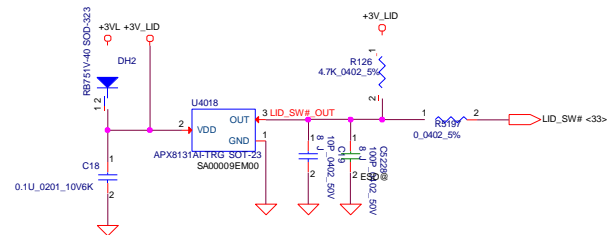




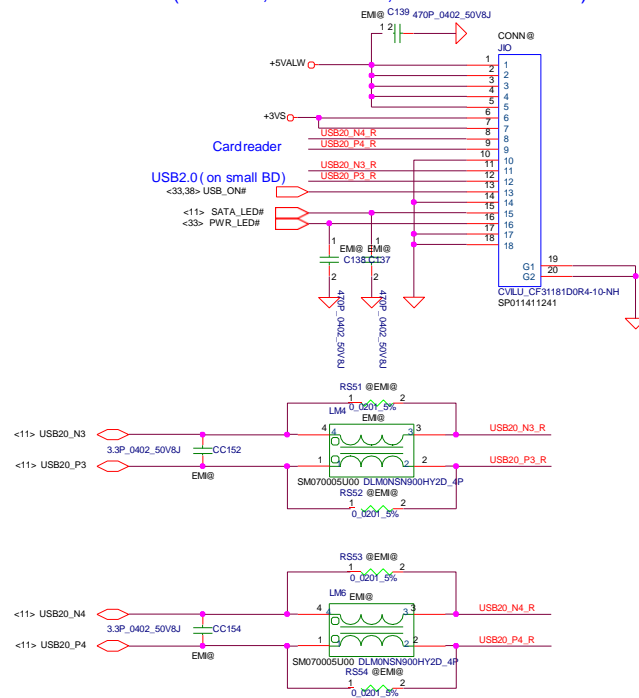
ESD Diode



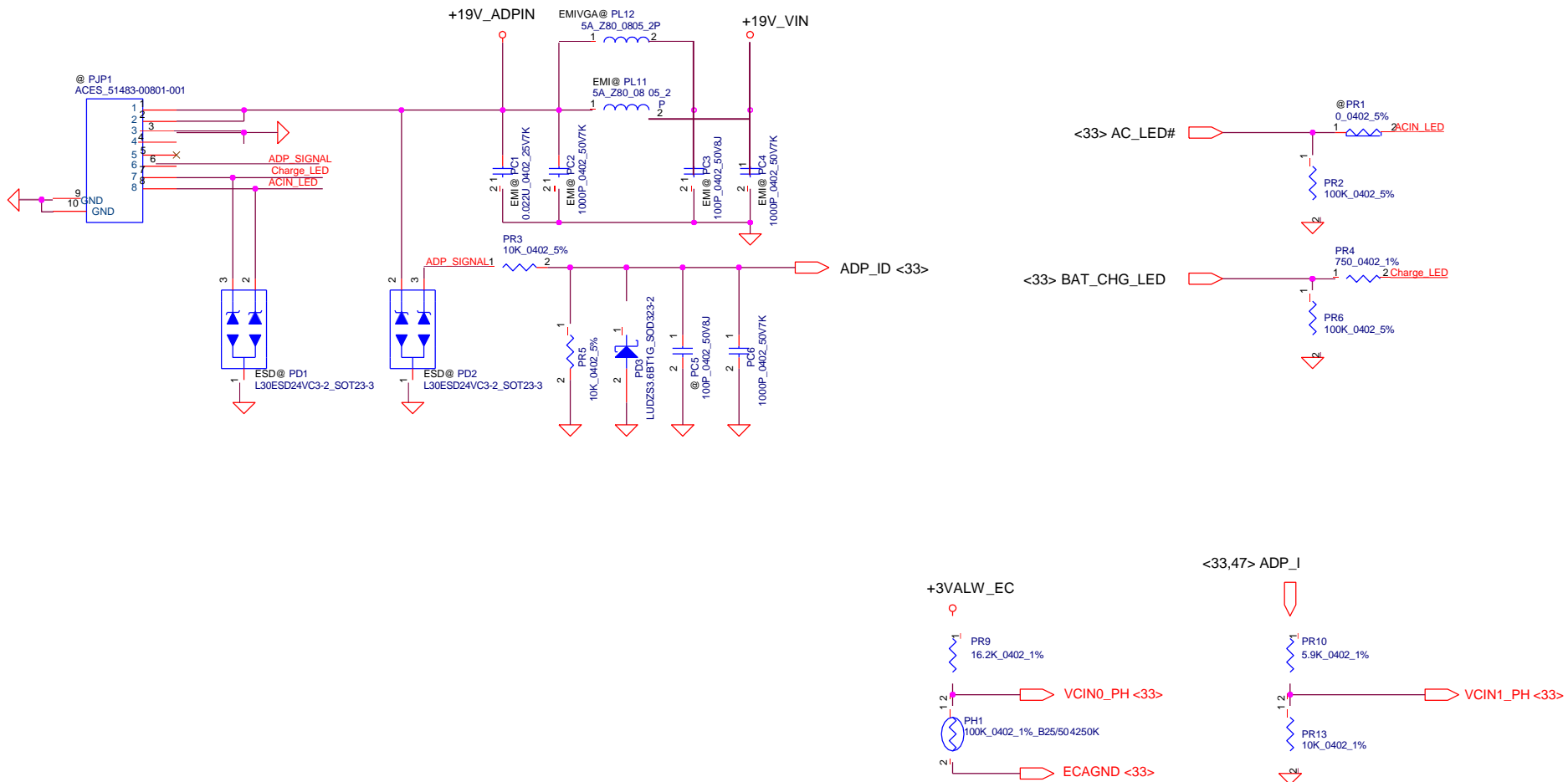
Lid Switch (Hall Effect Sensor)



IO BD Connector (USB2.0,Card reader,HDD & PWR LED)

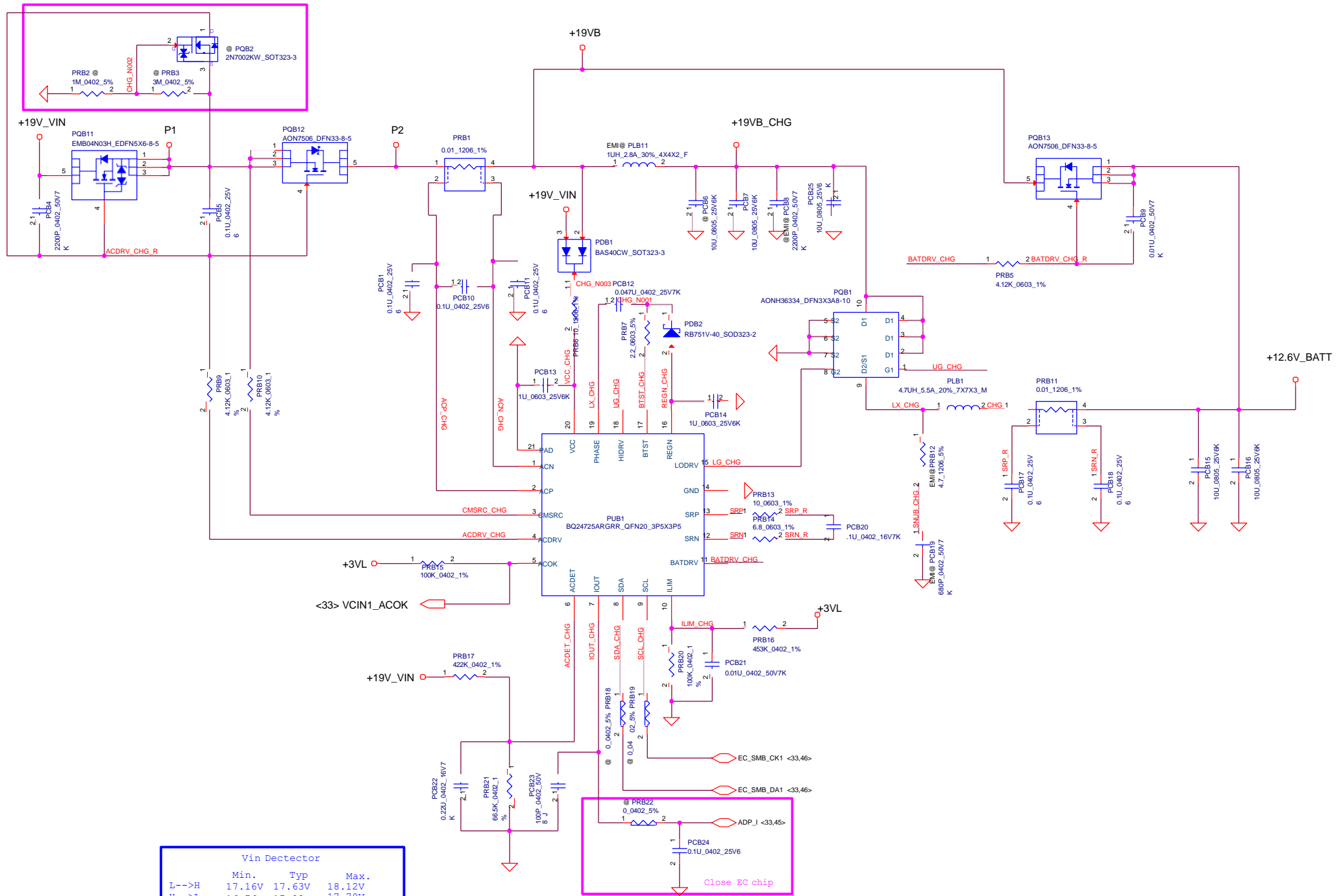


| | | | | |
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| Date | | | | Sheet 39 of 50 |
| Tuesday, January 09, 2018 | | | | EPK50_LA-G07CP |



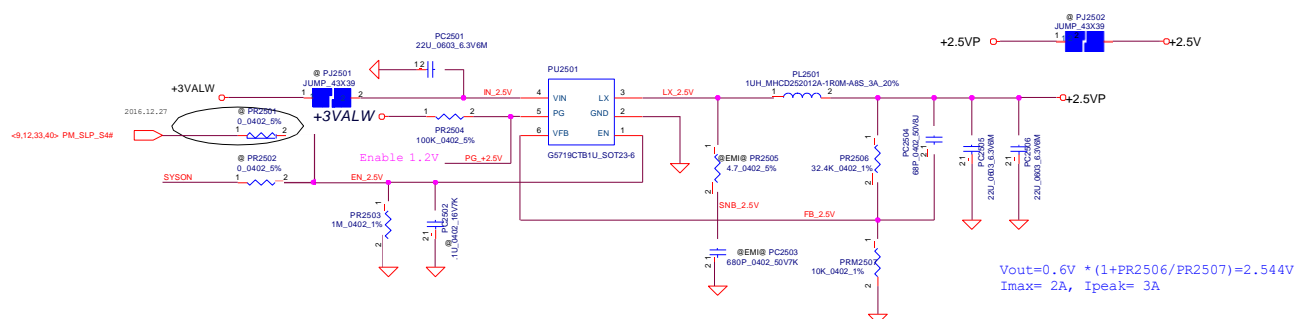
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| IssuedDate | 2016/09/01 | DecipheredDate | 2019/09/01 | Title | DCConn |
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| | | | | Date | Friday, January 05, 2018 |
| | | | | Sheet 45 | of 59 |

Protection for reverse input

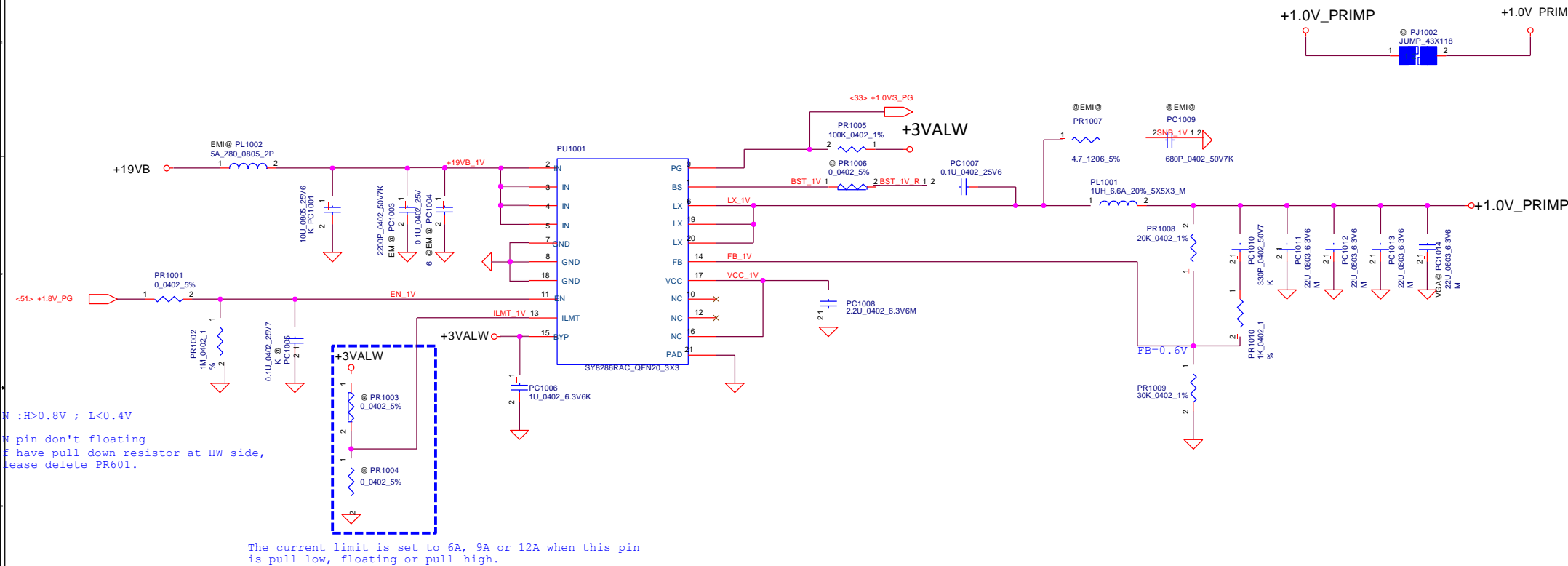


| Vin Detector | | | |
|----------------------------------|--------|--------|--------|
| | Min. | Typ | Max. |
| L-->H | 17.16V | 17.63V | 18.12V |
| H-->L | 16.76V | 17.22V | 17.70V |
| VILIM = 20*ILIM*Rsr | | | |
| ILIM = 3.3*100/(100+620)/20/0.02 | | | |
| = 2.291 A | | | |

| | | | | |
|---|--------------------|-----------------|--------------------------|----------|
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| Date: Friday, January 05, 2018 | | | | Rev v0.3 |
| Sheet 47 of 59 | | | | |



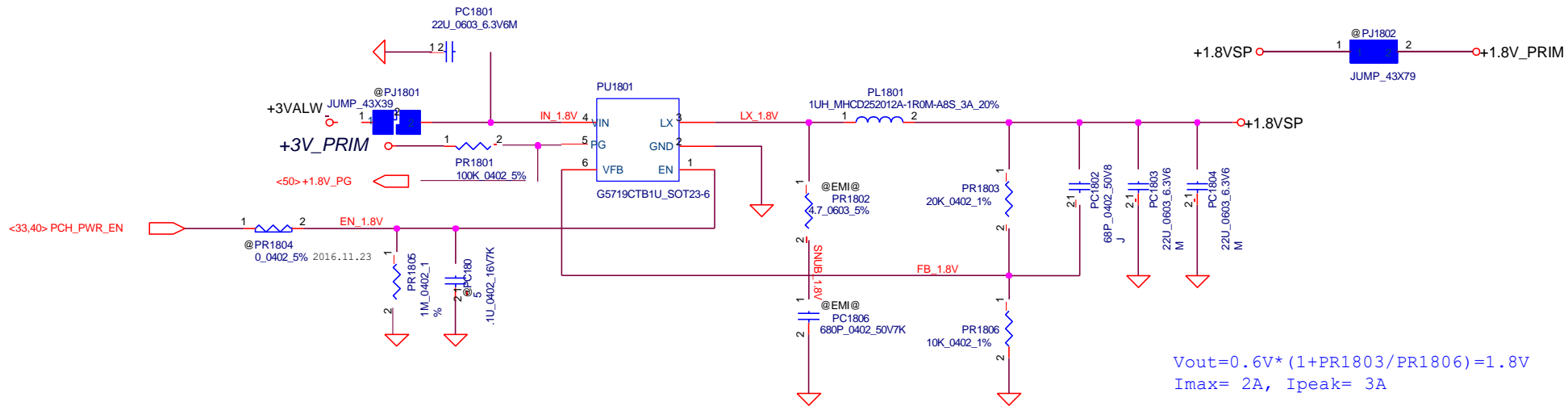
| | | | | |
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| Doc. No. | Rev. No. | | Issue Date | Sheet of |
| | | | Friday, January 05, 2018 | 59 |



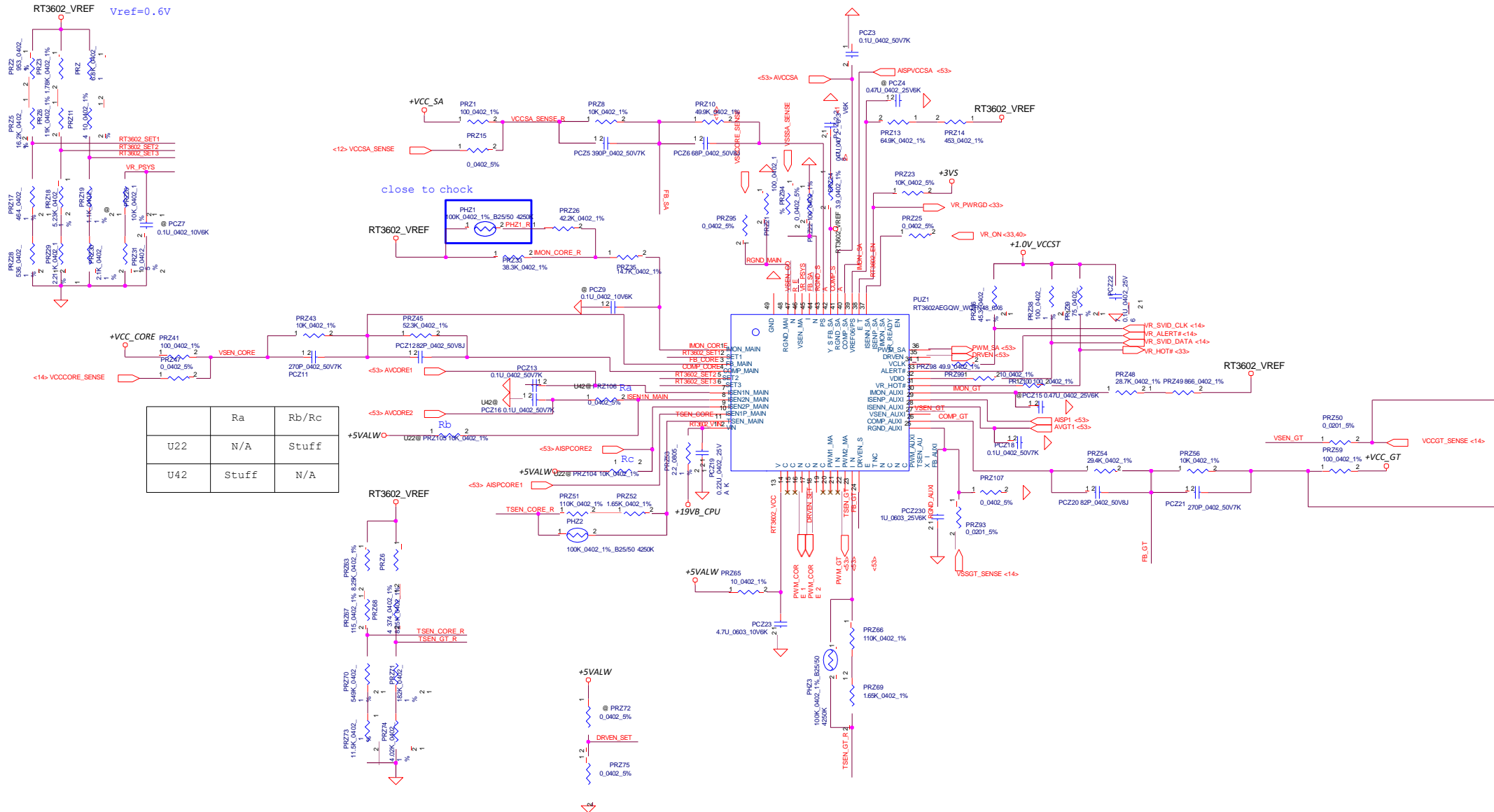
W :H>0.8V ; L<0.4V
 W pin don't floating
 F have pull down resistor at HW side,
 lease delete PR601.

The current limit is set to 6A, 9A or 12A when this pin
 is pull low, floating or pull high.

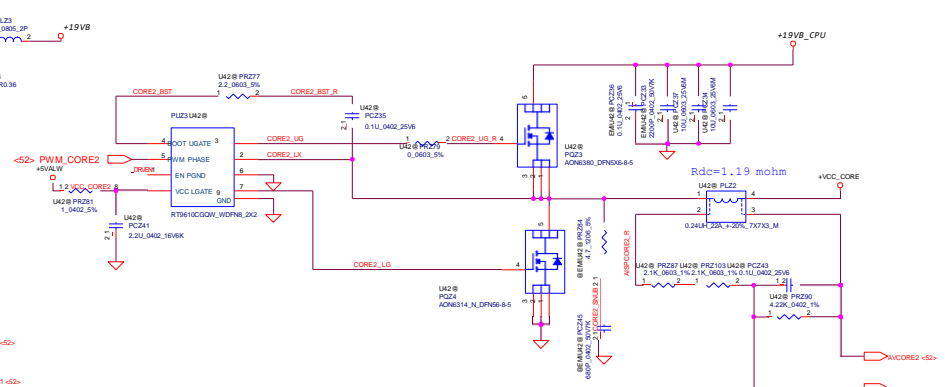
| | | | | |
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| Security Classification | Compal Secret Data | | | Title |
| Issued Date | 2016/09/01 | Deciphered Date | 2019/09/01 | 1.0V_PRIM |
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| | | | | Date: | Rev v0.3 |
| | | | | Sheet | 51 of 59 |



| | Ra | Rb/Rc |
|-----|-------|-------|
| U22 | N/A | Stuff |
| U42 | Stuff | N/A |



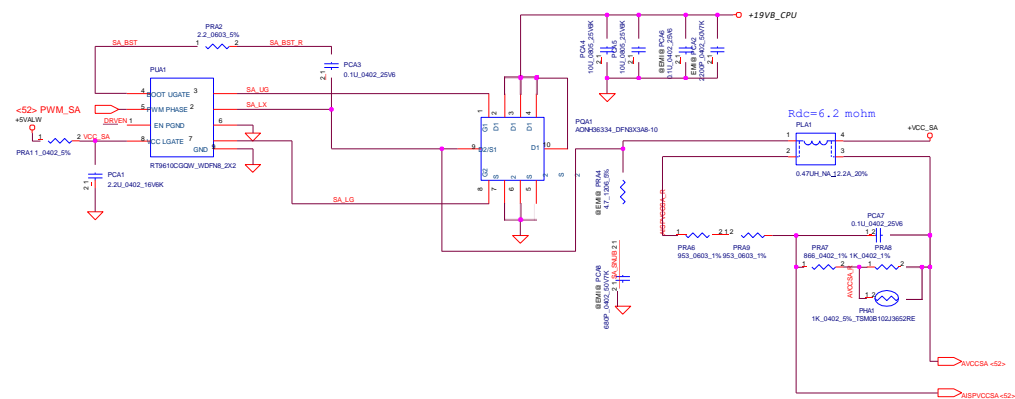
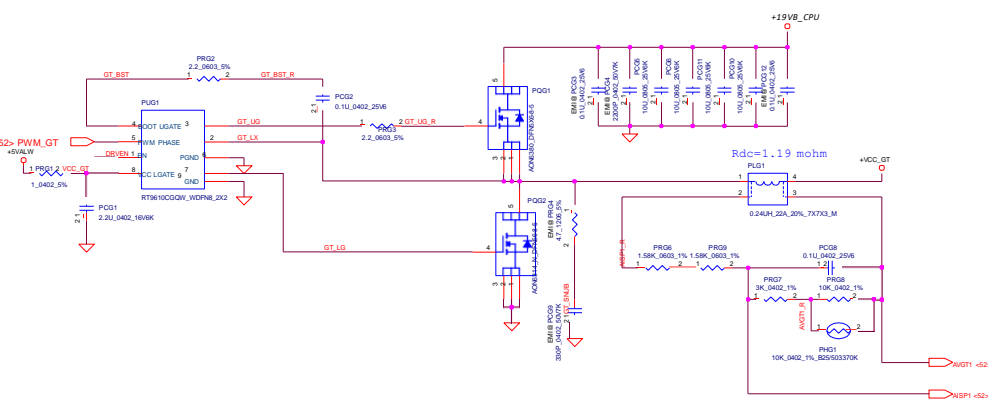
VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

```
U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A
```

```

042
LL=10.3 mohm
TDC=
ICCMAX=5A
OCP=9.5A

```



| | | | | |
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